



CPC307

PC/104-*Plus* Vortex86DX Based CPU Module

User Manual

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Revision Record

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Notation Conventions



Warning, ESD Sensitive Device!

This symbol draws your attention to the information related to electro static sensitivity of your product and its components. To keep product safety and operability it is necessary to handle it with care and follow the ESD safety directions.



Warning!

This sign marks warnings about hot surfaces. The surface of the heatsink and some components can get very hot during operation. Take due care when handling, avoid touching hot surfaces!



Caution: Electric Shock!

This symbol warns about danger of electrical shock (> 60 V) when touching products or parts of them. Failure to observe the indicated precautions and directions may expose your life to danger and may lead to damage to your product.



Warning!

Information marked by this symbol is essential for human and equipment safety. Read this information attentively, be watchful.



Note...

This symbol and title marks important information to be read attentively for your own benefit.



General Safety Precautions

This product was developed for fault-free operation. Its design provides conformance to all related safety requirements. However, the life of this product can be seriously shortened by improper handling and incorrect operation. That is why it is necessary to follow general safety and operational instructions below.



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Warning!

When handling this product, special care must be taken not to hit the heatsink (if installed) against another rigid object. Also, be careful not to drop the product, since this may cause damage to the heatsink, CPU or other sensitive components as well.

Please, keep in mind that any physical damage to this product is not covered under warranty.



Note:

This product is guaranteed to operate within the published temperature ranges and relevant conditions. However, prolonged operation near the maximum temperature is not recommended by Fastwel or by electronic chip manufacturers due to thermal stress related failure mechanisms. These mechanisms are common to all silicon devices, they can reduce the MTBF of the product by increasing the failure probability. Prolonged operation at the lower limits of the temperature ranges has no limitations.



Caution, Electric Shock!

Before installing this product into a system and before installing other devices on it, always ensure that your mains power is switched off.

Always disconnect external power supply cables during all handling and maintenance operations with this module to avoid serious danger of electrical shock.

Unpacking, Inspection and Handling

Please read the manual carefully before unpacking the module or mounting the device into your system. Keep in mind the following:



ESD Sensitive Device!

Electronic modules and their components are sensitive to static electricity. Even a non-perceptible by human being static discharge can be sufficient to destroy or degrade a component's operation! Therefore, all handling operations and inspections of this product must be performed with due care, in order to keep product integrity and operability:

- Preferably, unpack or pack this product only at EOS/ESD safe workplaces. Otherwise, it is important to be electrically discharged before touching the product. This can be done by touching a metal part of your system case with your hand or tool. It is particularly important to observe anti-static precautions when setting jumpers or replacing components.
- If the product contains batteries for RTC or memory back-up, ensure that the module is not placed on conductive surfaces, including anti-static mats or sponges. This can cause shortcircuit and result in damage to the battery and other components.
- Store this product in its protective packaging while it is not used for operational purposes.

Unpacking

The product is carefully packed in an antistatic bag and in a carton box to protect it against possible damage and harmful influence during shipping. Unpack the product indoors only at a temperature not less than +15°C and relative humidity not more than 70%. Please note, that if the product was exposed to the temperatures below 0°C for a long time, it is necessary to keep it at normal conditions for at least 24 hours before unpacking. Do not keep the product close to a heat source.

Following ESD precautions, carefully take the product out of the shipping carton box. Proper handling of the product is critical to ensure correct operation and long-term reliability. When unpacking the product, and whenever handling it thereafter, be sure to hold the module preferably by the front panel, card edges or ejector handles. Avoid touching the components and connectors.

Retain all original packaging at least until the warranty period is over. You may need it for shipments or for storage of the product.

Initial Inspection

Although the product is carefully packaged, it is still possible that shipping damages may occur. Careful inspection of the shipping carton can reveal evidence of damage or rough handling. Should you notice that the package is damaged, please notify the shipping service and the manufacturer as soon as possible. Retain the damaged packing material for inspection.

After unpacking the product, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Fastwel's official distributor from which you have purchased the product for additional instructions. Depending on the severity of the damage, the product may even need to be returned to the factory for repair. DO NOT apply power to the product if it has visible damage. Doing so may cause further, possibly irreparable damage, as well as result in a fire or electric shock hazard.

If the product contains socketed components, they should be inspected to make sure they are seated fully in their sockets.

Handling

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

In order to keep Fastwel's warranty, you must not change or modify this product in any way, other than specifically approved by Fastwel or described in this manual.

Technical characteristics of the systems in which this product is installed, such as operating temperature ranges and power supply parameters, should conform to the requirements stated by this document.

Retain all the original packaging, you will need it to pack the product for shipping in warranty cases or for safe storage. Please, pack the product for transportation in the way it was packed by the supplier.

When handling the product, please, remember that the module, its components and connectors require delicate care. Always keep in mind the ESD sensitivity of the product.

Three Year Warranty

Fastwel Co. Ltd. (Fastwel), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the currently established warranty period. Fastwel's only responsibility under this warranty is, at its option, to replace or repair any defective component part of such products free of charge.

Fastwel neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Fastwel shall have no liability for direct or consequential damages of any kind arising out of sale, delay in delivery, installation, or use of its products.

If a product should fail through Fastwel's fault during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.

Warranty period for Fastwel products is 36 months since the date of purchase.

The warranty set forth above does not extend to and shall not apply to:

- 1. Products, including software, which have been repaired or altered by other than Fastwel personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Fastwel.
- 2. Products, which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.

Returning a product for repair

- 1. Apply to Fastwel company or to any of the Fastwel's official representatives for the Product Return Authorization.
- 2. Attach a failure inspection report with a product to be returned in the form, accepted by customer, with a description of the failure circumstances and symptoms.
- 3. Carefully package the product in the antistatic bag, in which the product had been supplied. Failure to package in antistatic material will VOID all warranties. Then package the product in a safe container for shipping.
- 4. The customer pays for shipping the product to Fastwel or to an official Fastwel representative or dealer.

1 Introduction

This document presents general information on CPC307 CPU module, the details of its proper and safe installation, configuration and operation. The issues of PC/104 modules and external devices connection are also considered. This document applies to the module version 3.1.

1.1 Module Introduction

Fastwel CPC307 is designed for applications requiring high-performance low-power industrial controller with CAN interface. Fastwel CPC307 conforms to PC/104-Plus specification (except CPC307-01) and is compatible with a large number of peripheral and power supply modules delivered by a wide range of manufacturers.

Based on x86-compatible 32-bit Vortex86DX System-on-Chip (SoC) operating at 600 MHz, the module bears 256 MB soldered DDR2 memory and wide range of input/output interfaces. CPC307 allows system designers simple programming and provides portability of previously developed libraries for x86 architecture with DOS, Linux, Windows CE, and QNX support. Having two isolated CAN ports onboard along with a wide set of popular industrial interfaces, such as RS232, RS485, RS422, USB, and Fast Ethernet, CPC307 offers integrated functionality which is usually achieved by using several products from different manufacturers.

The module is designed for operation at temperatures from -40°C to +85°C.

CPC307 is supplied with the preinstalled FDOS 6.22 operating system and supports MS DOS 6.22, QNX 6.4, and Linux 2.6 operating systems.

1.2 CPC307 Versions

At the present time the CPC307 module is manufactured in several versions differing in interface capabilities.

Name	CPC307-01	CPC307-02	CPC307-03	CPC307-04	CPC307-05
Processor	Vortex86DX (600 MHz)				
RAM			256 MB		
Flash Disk	1 GB	1 GB	1 GB	_	1 GB
IDE	+	+	+	+	+
2xRS-232/485/422	+	+	+	+	+
2xRS-232	+	+	+	+	+
2xRS-422/485	+	+	-	+	+
2xCAN	+	+	-	+	+
LPT	+	+	+	+	+
4xUSB 2.0	+	+	+	+	+
PCI-104 Connector	-	+	+	+	+
LAN 10/100	-	+	+	+	+
8xGPIO	_	+	+	+	+
2xl2C	-	+	+	+	+
2xMicroSD	-	_	_	+	_
Coated	-	_	_	_	+
-50°C+90°C	-	_	_	-	+

Table 1.1:CPC307 Versions

Other options:

\COATED – Protective coating option for CPC307-01, -02, -03, -04;

\WCE5 – Preinstalled Windows CE 5.0 for CPC307-01, -02, -03, -05;

\LNX – Preinstalled Linux for CPC307-01, -02, -03, -05;

*For QNX 6.4, BSP can be provided.

1.3 Delivery Checklist

Table 1.2:	CPC307 Supplied Set
------------	---------------------

Name	Description
CPC30701 CPC30702 CPC30703 CPC30704 CPC30705	CPC307 processor module
ACS00023	DB9F to IDC2-10 2 mm adapter cable for connection to COM port (685611.082)
-	Mounting standoffs kit
-	Jumpers set
-	Antistatic bag and consumer carton box



Note:

Keep the antistatic bag and the original package at least until the warranty period is over. It can be used for future storage or warranty shipments.

1.4 Additional Accessories

Peripheral devices are attached to the module directly or via additional accessories and cables listed in the following table. Additional accessories are not supplied with the CPU module, are ordered separately.

Table 1.3:	CPC307 Additional Accessories	
------------	-------------------------------	--

Name	Description
CDM02	Adapter module for connection of 3.5" HDD or CD-ROM drive (469535.023)
ACS00010	FC44 cable for 2.5" HDD connection to 44-contact header
ACS00031-03 ACS0054	PHR-2 connector set. Includes JST PHR-2 socket and a set of contacts SPH-002T-P0.5S or connector with 0.5 m wires. Recommended counterpart connector for XP19 header (optoisolated Reset/IRQ) of the module (467941.016-02)
ACS00038 ACS00038-01 ACS00038-02	Connector set for connection of a power supply unit to the module. Includes AMP 4-171822-4 socket and a set of contacts 170262-1 (ACS00038) or a connector with 1.0 m wires (ACS00038-01, -02). Recommended counterpart connector for XP22 header (additional power connector)
ACS00040-01	Leotronics 2040-3102 socket (IDC2-10 2 mm). Recommended counterpart for XP5 (CAN), XP6 (COM3), XP7 (COM4), XP9 (LAN), XP10 (COM1), XP14 (GPIO), XP16 (COM2), XP17 (COM5,6) headers of the module
ACS00048, ACS00049, ACS00049-02	Leotronics socket, 10 positions, 2 mm pitch and contacts set (ACS00049) or contacts with 1 m wires (ACS00049-02) Recommended counterpart for XP5 (CAN), XP6 (COM3), XP7 (COM4), XP9 (LAN), XP10 (COM1), XP14 (GPIO), XP16 (COM2), XP17 (COM5,6) headers of the module
ACS00040-05	Leotronics IDC2-44 2 mm socket. Recommended counterpart for XP12 (LPT, USB), XP13 (IDE) headers of the module
ACS00048-04, ACS00049, ACS00049-02	Leotronics socket, 44 positions, 2 mm pitch and contacts set (ACS00049) or contacts with 1 m wires (ACS00049-02). Recommended counterpart for XP12 (LPT, USB), XP13 (IDE) headers of the module
ACS00042	Null modem cable

Fastwel

Name	Description	
ACS00043-01	PS/2 cable. Recommended counterpart for XP23 header of the module	
ACS00051 Cable for connection of two standard USB devices to XP12 (LPT/USB) connect		

2 **Technical Specifications**

2.1 General

- Form-factor:
 - PC/104-Plus
- CPU: Integrated in DM&P Vortex86DX SoC
 - 600 MHz
 - 32-bit x86 compatible core
 - 16-bit memory bus
 - Math coprocessor
 - 32 KB L1, 256 KB L2 cache
 - 6-stage pipeline
- System memory:
 - 256 MB soldered DDR2 SDRAM
 - DDR333
- IDE port:
 - One IDE channel (Primary)
 - For CPC307-04: support for up to two UltraDMA-100 IDE devices if the microSD sockets are not populated
 - For all other versions one IDE device can be connected
- Solid State Disk (except for CPC30704)
 - Soldered
 - 1 GB NAND flash
 - IDE interface
 - Can be used as bootable device
 - MS DOS-compatible Fastwel file system
- SD controller (for CPC30704 only):
 - Up to two microSD cards (bottom side sockets)
 - Up to 4 GB each card
- PS/2:
 - PS/2 keyboard and mouse interface
- Remote Reset/IRQ:
 - Discrete remote reset/interrupt input
 - 500V optoisolation
- USB:
 - Four USB 2.0 channels
 - One device can be connected to each channel



- LAN:
 - One Fast Ethernet port 10/100 Mbit/s (except for CPC30701)
 - 500 V isolation
- Serial ports:
 - Six serial ports (four for CPC30703)
 - High speed NS16C550 compatible
 - COM1, COM2: RS232/422/485, complete, up to 115.2 Kbaud
 - COM3, COM4: RS232, complete, up to 115.2 Kbaud
 - COM5, COM6: RS422/485, up to 3.6 Mbaud, 500 V isolation (except for CPC307-03)
 - Console operation via COM1 ... COM4
- CAN:
 - 2xCAN 2.0b (except for CPC307-03)
 - SJA1000T controller
 - Up to 1 Mbit/s
 - 500 V isolation
- Parallel port:
 - SPP/ECP/EPP compatible
- Expansion buses:
 - PCI and ISA
- Redundancy support
- GPIO:
 - 8 discrete I/O lines
- I2C:
 - 2 ports, via GPIO port
- Three watchdog timers:
 - One with fixed timeout period of 1.6 s
 - Two integrated in Vortex86DX with programmable timeout period
- Flash BIOS:
 - Main BIOS: 512 KB, soldered
 - Reserve: 256 KB, integrated in the controller
 - In-system modification
 - Automatic switching
- RTC:
 - On-board real time clock with Li battery backup
- Safety:
 - System configuration settings stored in CMOS + Serial FRAM (256 Kb)
 - Possibility of batteryless operation
- Software support:
 - AMI BIOS
 - Support for MS DOS 6.22, FreeDOS, Windows CE 5.0, Linux 2.6, QNX 6.4 operating systems

2.2 Power Requirements

The module can be powered via PC/104-Plus connectors. Additionally, power can be supplied via XP22 (4-contact AMP 4-171826-4) power connector by an external DC power source. Power supply unit should provide starting current, which is 2.1 A for CPC307-02 version. It is allowed to use power supply units with current limiting not less than 1.2 A. Selecting a power supply unit, the starting current should be considered as well as the consumption current of expansion modules.

Consumption current typical valuation is 0.6 A.

Connectors	Power Voltage	Voltage Limits	Consumption current	Starting current
PC/104 and PCI-104	+5 V	From +4.75V to +5.25V	1 A	1.5 A (0.5 ms)
XP22	+5 V	From +4.8V to +5.3V	1 A	1.5 A (0.5 ms)

Table 2.1: Power Supply Requirements



Important:

Please, find important notes on power supply in <u>subsection 3.2.17</u> of this document.

2.3 Environmental

- Operating temperature range: -40°C to +85°C (-50°C to +90°C for CPC30705)
- Storage temperature: –55°C to +90°C
- Relative humidity: up to 80% at 25°C, noncondensing



Note:

Protective coating of CPC307 versions makes them resistant to damp heat cyclic exposure at temperatures up to $+55\pm2^{\circ}$ C and relative humidity of up to $93\pm3\%$.

2.4 Mechanical

- Vibration (5 ... 2000 Hz) 10g;
- Single shock, peak acceleration 150 g;
- Multiple shock, peak acceleration 50 g.

If the module is operated in harsh environment, it is recommended to additionally fix counterpart connectors and cables.

2.5 Dimensions and Weight

- Dimensions, not more: 101.5 × 90.6 × 23.7 mm (4" × 3.57" × 0.93") (see also <u>Overall and Mounting Dimensions</u> for details)
- Weight:

Version	Net Weight, kg	Gross Weight, kg
CPC307-01	0.120	0.260
CPC307-02	0.125	0.265
CPC307-03	0.120	0.260
CPC307-04	0.125	0.265
CPC307-05	0.135	0.275

2.6 MTBF

MTBF for CPC307 is 200000 hours.

The value is calculated according to: Telcordia Issue 1 model, Method I Case 3, for continuous operation at a surface location, at normal environmental conditions and at ambient temperature $30 \,^{\circ}$ C.

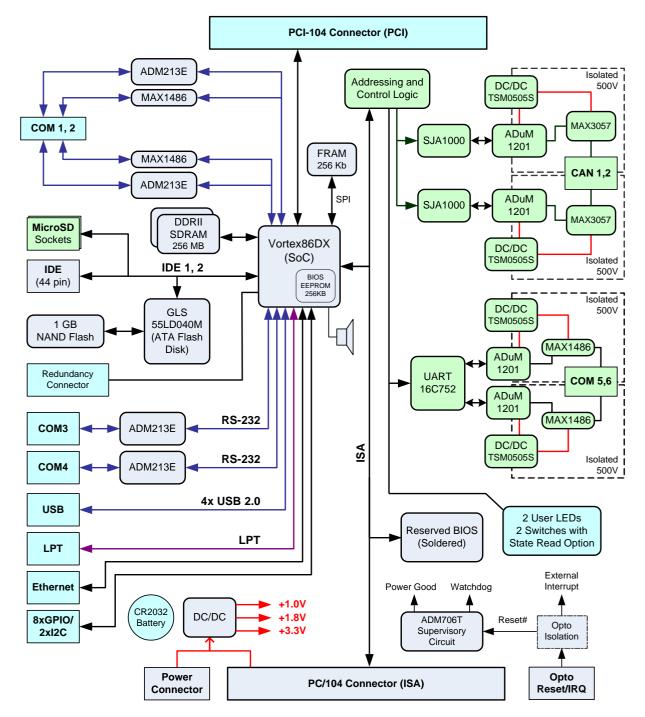


3 Functional Description

3.1 Structure and Layout

Functional diagram of the CPC307 module is shown in Figure 3.1.

Figure 3.1: CPC307 Block Diagram





CPC307 includes the following main functional units:

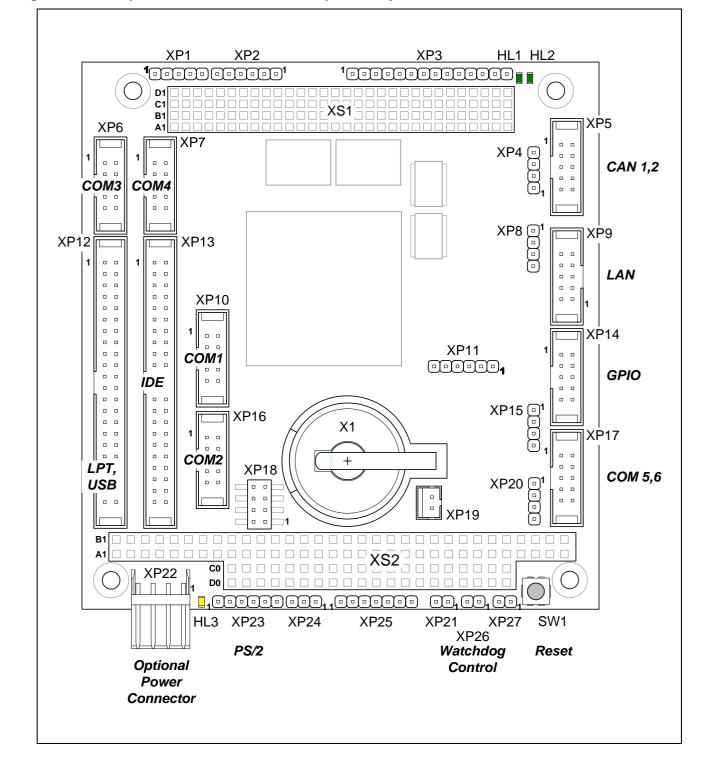
- SoC Vortex86DX
- 256 MB soldered DDR2 SDRAM system memory;
- IDE port with support for up to two UltraDMA/100 devices;
- SD controller (IDE, for CPC307-04 only);
- Onboard NAND flash-disk, 1 GB (IDE; except for CPC307-04);
- PS/2 keyboard/mouse port;
- Optoisolated (500V) remote Reset/interrupt input;
- Four USB 2.0 channels;
- Fast Ethernet port, 10/100 Mbit/s, 500V isolation (except for CPC307-01);
- Serial ports:
 - COM1, COM2: RS232/422/485, up to 115.2 Kbaud, complete;
 - COM3, COM4: RS232, up to 115.2 Kbaud, complete;
 - COM5, COM6: RS422/485, up to 3.6 Mbaud, 500V isolation (except for CPC307-03)
 - Console operation via COM1 ... COM4
- CAN:
 - Two CAN 2.0b ports (except for CPC307-03), SJA1000T controller; Up to 1 Mbit/s; 500 V isolation
- Parallel port, SPP/ECP/EPP compatible
- PCI and ISA expansion buses
- Redundancy support
- GPIO: 8 discrete I/O lines
- I2C: 2 ports, via GPIO port
- Three watchdog timers:
 - One with fixed timeout period of 1.6 s
 - Two integrated in Vortex86DX with programmable timeout period
- Flash memory based reserved BIOS, in-system modification;
- Real time clock with Li battery backup;
- CMOS+SFRAM (32 KB) for BIOS configuration storage;

Layouts of main CPC307 components and connectors on top and bottom sides are presented in Figures 3.2 and 3.3 respectively.

External connections are illustrated in <u>Chapter 4</u>.

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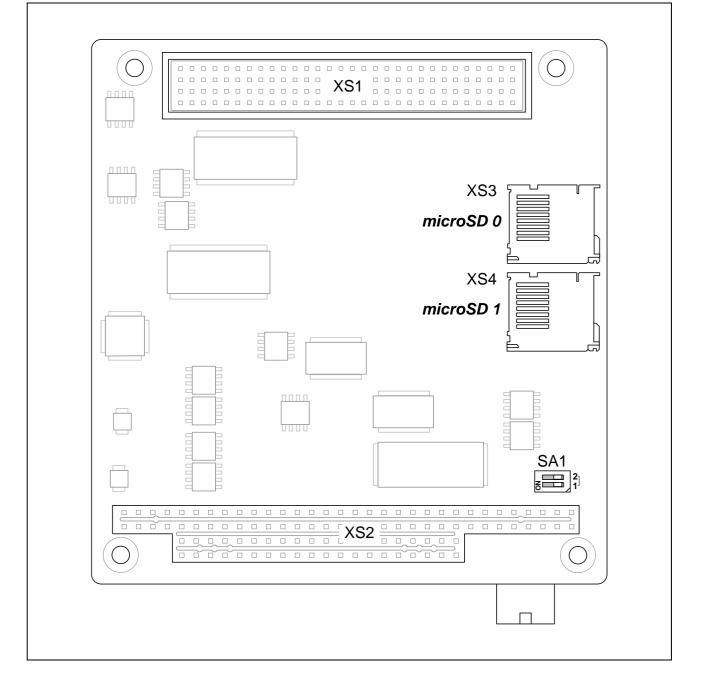
The layout may slightly differ for various versions of the module.







Bottom Side: Connectors and Main Components Layout (CPC30704)



The layout may slightly differ for various versions of the board.

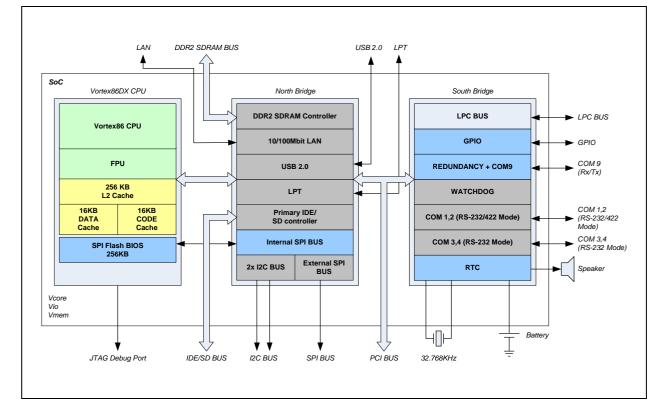
3.2 Functional Description

3.2.1 Vortex86DX SoC

DM&P Vortex86DX includes the following main functional units:

- 32-bit x86 compatible core operating at 600 MHz;
- 32 KB L1, 256 KB L2 cache;
- Math coprocessor;
- 16-bit DDR2 SDRAM memory bus;
- IDE/SD controller;
- Five RS-232 serial ports;
- Universal parallel port;
- Four USB 2.0 ports;
- PS/2 keyboard/mouse port;
- PCI, ISA, LPC, and SPI bus controllers;
- Two I2C interfaces;
- Built-in Ethernet 10/100 controller;
- RTC;
- CMOS memory for configuration storage;
- Integrated flash-memory for BIOS storage;
- Integrated redundancy system;
- Two programmable watchdog timers.

Figure 3.4: Vortex86DX SoC Block Diagram



Fastwel

3.2.2 SDRAM Memory

Two DDR2 SDRAM memory chips operating at 266 MHz are soldered on board. Total memory size is 256 MB.

3.2.3 IDE Interface

One-channel IDE controller allows connection of up to two IDE devices. UDMA-100 mode is supported.

If soldered NAND flash disk is enabled, one external device can be connected to XP13. If the onboard flash disk is disabled, two external drives can be connected as illustrated in the following table.

Table 3.1:	IDE Channel: Devices Connection Variants

Onboard Flash Disk	XP13 (Primary IDE)	XS3, XS4 (microSD 1, 2)
Enabled	One device	No connection
Disabled	Two devices	No connection
Disabled	No connection	Two devices



Important:

Before connecting external devices to CPC307-04 make sure that no microSD slot is populated and "IDE" mode is selected for Primary IDE in BIOS Setup. Simultaneous connection of external IDE devices and microSD cards is not allowed.

Figure 3.5: XP13 IDC44 Pins Numbering

XP13 is 2 mm pitch 2-row IDC44 pin header (Leotronics 4446-3440). Its pinout is presented in the table below. Recommended counterpart is Leotronics 2040-3442 socket for ribbon cable or Leotronics 2067-2442 socket and 2066-2000 contacts set.

Pin#	Signal	Pin#	Signal	Pin#	Signal	Pin#	Signal
1	/RESET	12	DD12	23	/IOW	34	-
2	GND	13	DD2	24	GND	35	DA0
3	DD7	14	DD13	25	/IOR	36	DA2
4	DD8	15	DD1	26	GND	37	/CS1
5	DD6	16	DD14	27	/IOCHRDY	38	/CS3
6	DD9	17	DD0	28	GND	39	DASP
7	DD5	18	DD15	29	/DACK	40	GND
8	DD10	19	GND	30	GND	41	+5V
9	DD4	20	-	31	IRQ	42	+5V
10	DD11	21	DRQ	32	/CS16	43	GND
11	DD3	22	GND	33	DA1	44	_

Table 3.2:XP13 Connector Pinout (IDE)

The ACS00010 (FC44) cable allows direct connection of a 2.5" HDD to the XP13 connector. Other IDE devices (3.5" HDD, CD-ROM) having 40-contact 2.54 mm pitch connector can be connected to CPC307 via the CDM02 (469535.023) adapter. This adapter is plugged directly to the 40-contact connector of the IDE device, and with ACS00010 cable is connected to XP13 connector of CPC307.



The operation modes of external IDE devices are set using jumpers on these devices.

3.2.4 MicroSD

Two microSD cards can be connected to CPC307-04 using XS3 (channel 0) and XS4 (channel 1) sockets on the bottom side (Hirose DM3B-DSF-PEJ).



Important:

Before connecting microSD cards to CPC307-04 make sure that no external devices are connected to XP13 header and "SD" mode is selected for Primary IDE in BIOS Setup. Simultaneous connection of external IDE devices and microSD cards is not allowed.

Figure 3.6: MicroSD Cards Contacts Numbering



Only microSD μ microSDHC formats are supported. The pinout of the XS3 and XS4 sockets is presented in the following table.

Table 3.3: XS3 and XS4 MicroSD Sockets Pinout

Pin #	Function	Pin #	Function
1	DAT2	6	GND
2	CD/DAT3	7	DAT0
3	CMD	8	DAT1
4	VCC (+3.3V)	9	CDSwA
5	CLK	10	CDSwB (GND)

3.2.5 ATA Flash Disk

CPC307 has ATA flash disk controller connected to Primary IDE interface. The capacity of the soldered on-board NAND flash memory chip is 1 GB (except for CPC30704). The system detects this controller as an IDE disk which can be used as bootable. NAND flash disk contains the preinstalled FDOS 6.22 operating system compatible with MS DOS 6.22 and some software utilities providing operational availability of the module.

Closing contacts 1-2 of XP24 sets master mode for the controller; slave mode is set by removing jumper from these contacts. The controller can be disabled by closing contacts 2-3 of XP24.

3.2.6 PS/2 Keyboard and Mouse Interface

PS/2 keyboard and mouse interface is routed to XP23 6-pin 2 mm pitch header (PLS2-40/6).

XP23 Connector Contacts Numbering

1 6 ••••••

Figure 3.7:

To make a custom cable it is recommended to use as a counterpart connector Leotronics 2018-3061 socket with 2023-2000 contacts.

The following table shows pinout of CPC307 XP23 connector.

Table 3.4: XP23 Contacts Designation

Pin Number	Signal	Pin Number	Signal
1	KBD CLK	4	GND
2	KBD DATA	5	+5V
3	MOUSE CLK	6	MOUSE DATA

3.2.7 Optoisolated Reset/IRQ Input

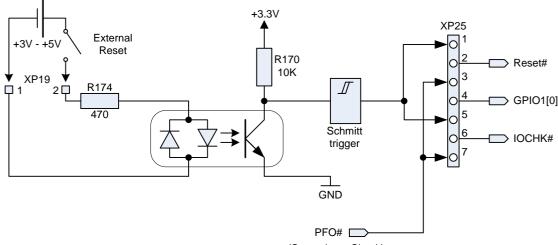
Figure 3.8: XP19 Connector



XP19 is a 2-pin 2 mm pitch header (JST B 2B-PH-KL) that is intended for connection of a remote Reset/IRQ signal source with voltage of 3 to 5 V. The discrete input has 500 V optoisolation.

Recommended counterpart is JST PHR-2 socket and SPH-002T-P0.5S contacts for crimping.

Figure 3.9: Discrete Input Optoisolation and Reset or IRQ Source Selection



(Supervisory Circuit)

Depending on position of jumpers of XP25 pin header, the input is connected to different circuits:

- Closing contacts 1-2 of XP25 enables Reset on input;
- Closing contacts 4-5 of XP25 connects input to line 0 of GPIO1 port. Selection Reset function or IRQ line number is possible in BIOS Setup utility or by programming registers of GPIO1 port.
- Closing contacts 5-6 of XP25 enables NMI interrupt generation on input. This position of jumper connects the input to IOCHK# line of ISA bus.



XP25 pinpad also allows to set function of PFO# signal (Power Fail Output) from Power voltage supervisor chip. PFO# signal is set to "0" on +5V voltage drop down to +4.75V. PFO# signal is connected to the following circuits:

- Closing contacts 2-3 of XP25 enables Reset on active PFO# level;
- Closing contacts 3-4 of XP25 connects PFO# to line 0 of GPIO1 port. Selection of Reset function or IRQ line number on PFO# is possible in BIOS Setup utility or by programming registers of GPIO1 port.
- Closing contacts 6-7 of XP25 enables NMI interrupt generation on PFO#. This position of jumper connects PFO# signal to IOCHK# line of ISA bus.

See also "<u>Configuration Jumpers</u>" and "<u>GPIO Ports</u>" sections of this document.



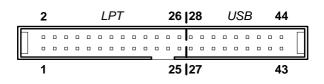
The module is equipped with four USB 2.0 host ports routed to part of XP12 header contacts. Operation mode is selected in BIOS Setup. Each channel has separate power control and protection circuit (+5V, 500 mA). One USB device may be connected to each port.

USB drive boot is supported. Operation mode and boot priority is set in BIOS Setup. Every USB device requires compatibility check.

By default, USB flash drives with volume less than or equal to 512 MB are detected as FDD drive by system, drive names A:, B:. System does not support more than two FDDs at once.

XP12 is a 2-row pin header (Leotronics 2073-3442) with 2 mm pitch.

Figure 3.10: XP12Connector



USB devices can be connected to XP12 header using a custom adaptor cable with Leotronics 2040-3442 socket for ribbon cable or Leotronics 2022-2202 socket with 2023-2000 contacts.

Table 3.5:XP12 Connector Pinout (USB)

Pin Number	Signal	Pin Number	Signal
27	+5V (USB1)	28	+5V (USB2)
29	D1-	30	D2-
31	D1+	32	D2+
33	GND (USB1)	34	GND (USB2)
35	-	36	-
37	+5V (USB3)	38	+5V (USB4)
39	D3-	40	D4-
41	D3+	42	D4+
43	GND (USB3)	44	GND (USB4)

3.2.9 Fast Ethernet Interface

One Fast Ethernet channel (10/100 Mb/s) is available via XP9 connector on all versions of CPC307 except CPC30701. Ethernet controller is integrated in Vortex86DX SoC.

Figure 3.11: XP9 Connector



XP9 is a 2-row 2 mm pitch IDC10 header (Leotronics 2073-3102).

Recommended counterpart – 2040-3442 socket for ribbon cable or Leotronics 2022-2102 socket with 2023-2000 contacts.

Table 3.6: XP9 Ethernet Header Pinout

Pin Number	Signal	Pin Number	Signal
1	LAN1_TX+	6	NC
2	LAN1_TX-	7	NC
3	LAN1_RX+	8	NC
4	LAN1_RX-	9	NC
5	NC	10	NC

3.2.10 Serial Ports

Figure 3.12: IDC10 Pins Numbering



The CPC307 is furnished with six serial ports (CPC30703 with four).

3.2.10.1 COM1 and COM2

COM1 and COM2 ports operate in RS232 or RS485/422 modes and have standard PC AT base addresses. IRQ line and base address selection is performed in BIOS Setup. The operation mode for each port is set independently in BIOS Setup or via GPIO2 port. By default for RS232 mode is set COM1 and COM2.

Maximum transmission rate for these ports is 115.2 Kbaud; these ports are fully compatible with UART16550.

In RS485/422 mode transmitters are hardware controlled. Operation mode is selected independently for each port.

RS232 Mode

In RS232 mode the ports operate as complete 9-wire interface. RS232 mode is enabled for COM1 by setting line 0 of GPIO2 port to "1" and the line direction to "output"; for COM2 – by setting line 2 of GPIO2 port to "1" and the line direction to "output".

RS485/422 Mode

In RS485/422 mode transmitter is hardware controlled and receiver is constantly "on".



In RS485 mode (half duplex operation of RS485/422 converter) the lines TX+ and RX+ are connected in the driver, as well as TX- and RX- lines at the side of interface connector. In RS422 mode these lines are not connected and routed to the connector separately.

RS485 mode is enabled for COM1 by setting line 1 of GPIO2 port to "1"; for COM2 – by setting line 3 of GPIO2 port to "1". RS422 mode is enabled for COM1 by setting line 1 of GPIO2 port to "0"; for COM2 – by setting line 3 of GPIO2 port to "0". Line direction for lines 1 and 3 should be set to "output".

Figure 3.13: XP18 Pinpad

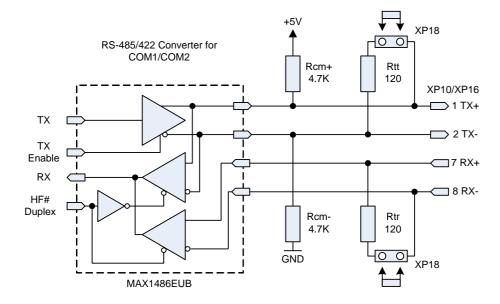
2468	
	120 (\pm 5%) Ohm terminating resistors for RS485/422 modes can be
	connected by setting appropriate jumpers on XP18 pinpad.
1 3 5 7	

Table 3.7:	XP18 Pinpad Jumpers
------------	---------------------

Closed Contacts	Connected Resistors
1-2	Rtt for TX-/TX+ lines of COM1
3-4	Rtr for RX-/RX+ lines of COM1
5-6	Rtt for TX-/TX+ lines of COM2
7-8	Rtr for RX-/RX+ lines of COM2

If RS485 network is inactive, all drivers are switched to the third state, therefore all nodes are in receive mode. Thus, the state of a network is not determined. If the potential difference between RX+ and RX– inputs of a receiver is less than ±200 mA threshold level, then the receiver output (RX) logical level will be equal to the last received data bit. To provide proper voltage level in the network inactive state, protective bias resistors are used. To set the initial high voltage level at TX+ line, a 4.7 kilohm bias resistor (Rcm+) is installed. To set the initial low voltage level at TX– line, a 4.7 kilohm bias resistor (Rcm-) is installed as shown in the figure below.

Figure 3.14: RS485/422 Transmitter with Bias Elements and Terminating Resistors



COM1 and COM2 are routed to XP10 and XP16 connectors respectively (IDC2-10, 2-row, 2 mm pitch connectors, Leotronics 2073-3102). Recommended counterparts are Leotronics 2040-3102 socket for ribbon cable or Leotronics 2022-2102 socket with 2023-2000 contacts.



Important:

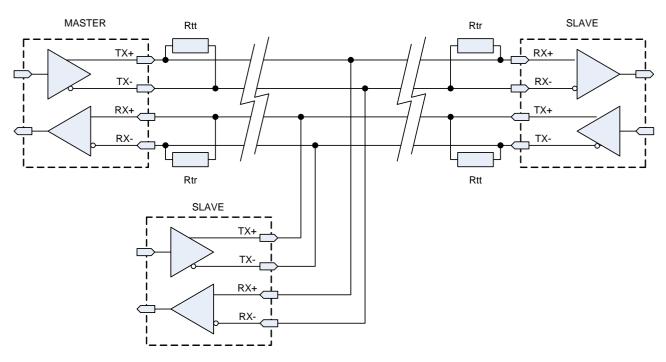
+5V lines are protected by 0.5A fuse. Recommended consumption current for connected external modules is 0.4A. It is not recommended to power more than one external module via interface connectors in order not to overload power circuits of CPC307.

The following table shows pins designation for XP10 and XP16 headers.

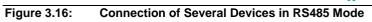
Table 3.8:	XP10 and XP16 Pin Assignments
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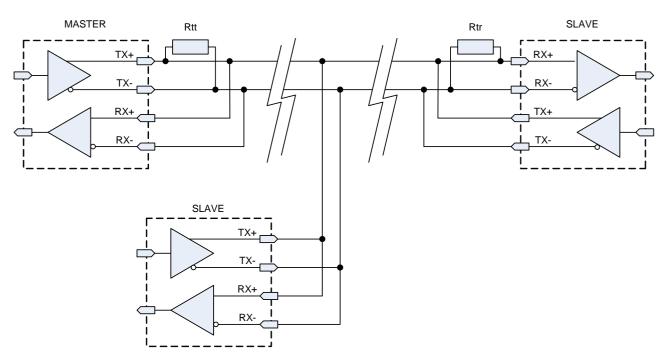
Pin #	Signal		Pin #	Signal				
4	DCD	(RS-232)	2	DSR	(RS-232)			
1	TX+	(RS-422/485)	2	TX- (RS-422)	(RS-422/485)			
3	RXD#		4	RTS				
5	TXD#		6	CTS				
7	DTR (RS-232)		8	RI	(RS-232)			
7	RX+	(RS-422/485)	0	RX-	(RS-422/485)			
9	GND		10	+5V				

Figure 3.15: Connection of Several Devices in RS422 Mode









COM3 (XP6) and COM4 (XP7) ports operate in 9-wire RS232 mode and have standard PC AT base addresses. IRQ line and base address selection is performed in BIOS Setup. Maximum transmission rate for these ports is 115.2 Kbaud; they are fully compatible with UART16550.

Both connectors are 2-row, 2 mm pitch pin headers (Leotronics 2073-3102). Recommended counterparts are Leotronics 2040-3102 socket for ribbon cable or Leotronics 2022-2102 socket with 2023-2000 contacts.



Important:

+5V lines are protected by 0.5A fuse. Recommended consumption current for connected external modules is 0.4A. It is not recommended to power more than one external module via interface connectors in order not to overload power circuits of CPC307.

Table 3.9:XP6 and XP7 Pin Assignments

Pin #	Signal	Pin #	Signal
1	DCD	2	DSR
3	RXD#	4	RTS
5	TXD#	6	CTS
7	DTR	8	RI
9	GND	10	+5V

3.2.10.3 COM5 and COM6

COM5 and COM6 ports operate in RS422/485 mode. Base addresses (BA) selection is performed by programming the Vortex86DX registers. Interrupt lines are set by hardware. For details see <u>Integrated</u> <u>Address Decoder</u> section of this document.

Maximum transmission rate for these ports is 3.6 Mbaud; they are fully compatible with UART16550.

Table 3.10: COM5 and COM6 Controllers Resources

	СОМ5	СОМ6
Control area	BA+0x00 – BA+ 0x07	BA+0x08 – BA+ 0x0F
ISA interrupt lines	IRQ7	IRQ9

Operation mode for each port is set by programming the registers of EXAR XR16C2850IM controller. Transmitters in RS485/422 mode are hardware controlled.

To enable RS485 interface, the lines TX+ and RX+, as well as TX- and RX- should be connected at XP17 connector.

Figure 3.17: XP15 and XP20 Pinpads

XP15 XP20	
1 2 3 4 1 2 3 4	120 (\pm 5%) ohm terminating resistors for RS485/422
	modes can be connected by setting appropriate
	jumpers on XP15 and XP20 pinpads.



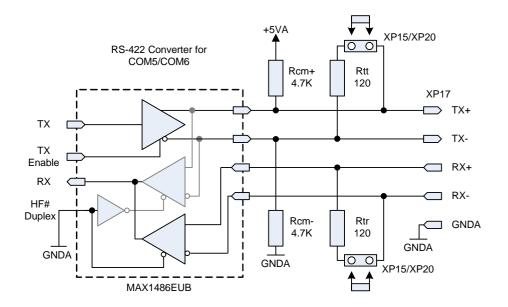
CPC307

Table 3.11: XP15 and XP20 Pinpads Jumpers

Closed Contacts	Connected Resistors
XP15: 1-2	Rtt for TX-/TX+ lines of COM5
XP15: 3-4	Rtr for RX-/RX+ lines of COM5
XP20: 1-2	Rtt for TX-/TX+ lines of COM6
XP20: 3-4	Rtr for RX-/RX+ lines of COM6

If RS485 network is inactive, all drivers are switched to the third state, therefore all nodes are in receive mode. Thus, the state of a network is not determined. If the potential difference between RX+ and RX- inputs of a receiver is less than ±200 mA threshold level, then the receiver output (RX) logical level will be equal to the last received data bit. To provide proper voltage level in the network inactive state, protective bias resistors are used. To set the initial high voltage level at TX+ line, a 4.7 kilohm bias resistor (Rcm+) is installed. To set the initial low voltage level at TX- line, a 4.7 kilohm bias resistor (Rcm-) is installed as shown in the figure below.

Figure 3.18: Transmitter with Protective Bias Elements and Terminating Resistors



COM5 and COM6 are routed to XP17 2-row, 2 mm pitch pin header (IDC2-10 Leotronics 2073-3102). Recommended counterparts are Leotronics 2040-3102 socket for ribbon cable or Leotronics 2022-2102 socket with 2023-2000 contacts. The pinout of XP17 is presented in a table below.



Pin #	Signal	Pin #	Signal
1	TX+ (COM5)	2	TX- (COM5)
3	RX+ (COM5)	4	RX- (COM5)
5	GND (COM5)	6	TX+ (COM6)
7	TX- (COM6)	8	RX+ (COM6)
9	RX- (COM6)	10	GND (COM6)

 Table 3.12:
 XP17 Pin Assignments (COM5 and COM6)

3.2.11 Parallel Printer Port (LPT)

LPT port is available via first 26 contacts of XP12 2-row 2 mm pitch connector (IDC2-20 Leotronics 2073-3442). LPT port of CPC307 supports SPP, EPP, and ECP operation modes and has standard PC/AT base addresses. Base address and interrupt line are selected in BIOS Setup.

Figure 3.19: XP12 Connector

2			2			LPT					2	6	2	8		l	US	SB		44		
		0				0		0	0		0		0			0	0		0			
	1											2	25	2	7						43	

Recommended counterpart connector for making a custom adaptor cable is Leotronics 2040-3442 socket for ribbon cable or Leotronics 2022-2442 socket with 2023-2000 contacts.



Important:

+5V lines are protected by 0.5A self-resettable switch. Recommended consumption current for connected external modules is 0.4A. It is not recommended to power more than one external module via interface connectors in order not to overload power circuits of CPC307.

The table below describes pin assignments of LPT part of XP12 connector.

Table 3.13:	XP12 (LPT) Connector Pinout	

Pin #	Signal	Pin #	Signal
1	STB#	2	AFD#
3	PD0	4	ERR#
5	PD1	6	INIT#
7	PD2	8	SLIN#
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND

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Pin #	Signal	Pin #	Signal					
23	PE	24	GND	1				
25	SLCT	26	+5V					

3.2.12 Expansion Buses: ISA and PCI

The module is equipped with two interface expansion headers stipulated by PC/104-Plus specification – 104-pin ISA and 120-pin PCI (except for CPC30701) connectors. They allow stacking up to four PC/104-Plus modules. Up to three PC/104-Plus PCI-master expansion modules are supported. Both connectors are available as a socket at the top side of the module and as a pin array with organizer at the bottom side of CPC307.

3.2.12.1 PCI Header

PC/104-Plus standard specifies availability of 120-pin (30x4) 2 mm header. This interface header accepts up to 3 stackable PC/104-Plus PCI bus mastering modules and carries all of the appropriate 32-bit 33 MHz PCI signals. PCI signals are available both via the socket at the top side of the module (XS1, AMP 1375799-1) and via a pin array with organizer (AMP 1375801-1) at the bottom side of CPC307.

XS1 contacts designation and load capacity (LC) are shown in the following table.

Figure 3.20: XS1 Connector Contacts Layout

ABCD	0 40 40 40 40 40 40 40 40 40 40 40 40 40	0D (0D (0D (0D (0D (
	~	8

Pin	Signal	State	LC, mA	Pin	Signal	State	LC, mA
A1	GND	Power	_	B1	_	_	_
A2	VI/O	+3.3V (Out)	-	B2	AD2	In / Out	12
A3	AD5	In / Out	12	B3	GND	Power	-
A4	C/BE0#	In / Out	12	B4	AD7	In / Out	12
A5	GND	Power	-	B5	AD9	In / Out	12
A6	AD11	In / Out	12	B6	VI/O	+3.3V (Out)	_
A7	AD14	In / Out	12	B7	AD13	In / Out	12
A8	-	-	-	B8	C/BE1#	In / Out	12
A9	SERR#	PU (10K)	_	B9	GND	Power	_
A10	GND	Power	-	B10	PERR#	PU (10K)	_
A11	STOP#	In / Out	12	B11	_	-	_
A12	_	_	-	B12	TRDY#	In / Out	12
A13	FRAME#	In / Out	12	B13	GND	-	_
A14	GND	Power	-	B14	AD16	In / Out	12
A15	AD18	In / Out	12	B15	-	_	-
A16	AD21	In / Out	12	B16	AD20	In / Out	12
A17	_	_	-	B17	AD23	In / Out	12
A18	IDSEL0	AD12	-	B18	GND	Power	-
A19	AD24	In / Out	12	B19	C/BE3#	In / Out	

 Table 3.14:
 XS1 Connector Contacts Designation (Rows A, B)



CPC307

Pin	Signal	State	LC, mA	Pin	Signal	State	LC, mA		
A20	GND	Power	_	B20	AD26	In / Out	12		
A21	AD29	In / Out	12	B21	+5V	Power	-		
A22	+5V	Power	-	B22	AD30	In / Out	12		
A23	REQ0#	In	-	B23	GND	Power	-		
A24	GND	Power	-	B24	REQ2#	In	-		
A25	GNT1#	Out	12	B25	VI/O	+3.3V (Out)	-		
A26	+5V	Power	-	B26	CLK0	Out	12		
A27	CLK2	Out	6	B27	+5V	In	-		
A28	GND	Power	-	B28	INTD#	In	-		
A29	+12V	-	_	B29	INTA#	In	-		
A30	-12V	-	_	B30	_	-	_		
100		ad Capacity		200					

Table 3.15: XS1 Connector Contacts Designation (Rows C, D)

Pin	Signal	State	LC, mA	Pin	Signal	State	LC, mA
C1	+5V	Power	–	D1	AD0	In / Out	12
C2	AD1	In / Out	12	D2	+5V	Power	_
C3	AD4	In / Out	12	D3	AD3	In / Out	12
C4	GND	Power	-	D4	AD6	In / Out	12
C5	AD8	In / Out	12	D5	GND	Power	_
C6	AD10	In / Out	12	D6	M66EN (GND)	-	-
C7	GND	Power	_	D7	AD12	In / Out	12
C8	AD15	In / Out	12	D8	-	-	-
C9	-	-	-	D9	PAR	In / Out	12
C10	-	-	_	D10	-	-	_
C11	LOCK#	PU (10K)	_	D11	GND	Power	_
C12	GND	Power	-	D12	DEVSEL#	In / Out	12
C13	IRDY#	In / Out	12	D13	-	-	_
C14	-	-	-	D14	C/BE2#	In / Out	12
C15	AD17	In / Out	12	D15	GND	Power	_
C16	GND	Power	_	D16	AD19	In / Out	12
C17	AD22	In / Out	12	D17	-	-	-
C18	IDSEL1	AD13	_	D18	IDSEL2	AD14	_
C19	VI/O	+3.3V (Out)	-	D19	IDSEL3	AD15	_
C20	AD25	In / Out	12	D20	GND	Power	-
C21	AD28	In / Out	12	D21	AD27	In / Out	12
C22	GND	Power	-	D22	AD31	In / Out	12
C23	REQ1#	In	_	D23	VI/O	+3.3V (Out)	_
C24	+5V	Power	-	D24	GNT0#	Out	12
C25	GNT2#	Out	12	D25	GND	Power	-
C26	GND	Power	-	D26	CLK1	Out	12
C27	CLK3	Out	6	D27	GND	Power	_
C28	+5V	Power	-	D28	RST#	Out	12
C29	INTB#	In	-	D29	INTC#	In	-
C30	GNT3#	PU (10K)	_	D30	GND	Power	_



Mada

Note:
In two tables above:
"–" – Not used;
"Power" – supplied to the stacked modules
In/Out column shows the data transfer direction for a processor
module being the bus master.

3.2.12.2 **ISA Header**

XS2 header mounted on CPC307 allows connection of PC/104 expansion modules via ISA bus (8/16bit, 8.3/16.6 MHz, DMA support). Master mode for peripheral modules is not supported. ISA signals are available both via the socket at the top side of the module (AMP 1375795-2) and via a pin array with organizer (AMP 1445251-1) at the bottom side of CPC307.

The contact configuration of XS2 header is shown in the figure below. The tables following the figure presents the designation of its contacts and load capacity.

Figure 3.21: **ISA Header Contacts Layout**

B1																		B32 A32
A1		I			囸	囸					囸		囸		I			A32
			C	0												6	C19	
			D	οl											I	ן נ	019	

Pin #	Signal	In/Out	LC, mA	Pin #	Signal	In/Out	LC, mA
A1	/IOCHK	-	_	B1	GND	Power	-
A2	SD7	In/Out	16	B2	RESET	Out	16
A3	SD6	In/Out	16	B3	+5V	Power	-
A4	SD5	In/Out	16	B4	IRQ9	In	_
A5	SD4	In/Out	16	B5	-5V	Power	_
A6	SD3	In/Out	16	B6	DRQ2	In	-
A7	SD2	In/Out	16	B7	-12V	Power	_
A8	SD1	In/Out	16	B8	0WS	In	-
A9	SD0	In/Out	16	B9	+12V	Power	_
A10	IOCHRDY	In	16	B10	GND	Power	_
A11	AEN	Out	16	B11	/SMEMW	Out	16
A12	SA19	Out	16	B12	/SMEMR	Out	16
A13	SA18	Out	16	B13	/IOW	Out	16
A14	SA17	Out	16	B14	/IOR	Out	16
A15	SA16	Out	16	B15	/DACK3	Out	8
A16	SA15	Out	16	B16	DRQ3	In	_
A17	SA14	Out	16	B17	/DACK1	Out	8
A18	SA13	Out	16	B18	DRQ1	In	_
A19	SA12	Out	16	B19	/REFRESH	Out	8
A20	SA11	Out	16	B20	BCLK	Out	8
A21	SA10	Out	16	B21	IRQ7	In	-
A22	SA9	Out	16	B22	IRQ6	In	-

Table 3.16: ISA XS2 Connector (Rows A and B) Contacts Designation

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					~ •		
Pin #	Signal	In/Out	LC, mA	Pin #	Signal	In/Out	LC, mA
A23	SA8	Out	16	B23	IRQ5	In	_
A24	SA7	Out	16	B24	IRQ4	In	-
A25	SA6	Out	16	B25	IRQ3	In	-
A26	SA5	Out	16	B26	/DACK2	Out	8
A27	SA4	Out	16	B27	TC	Out	8
A28	SA3	Out	16	B28	BALE	Out	16
A29	SA2	Out	16	B29	+5V	Power	-
A30	SA1	Out	16	B30	OSC	Out	16
A31	SA0	Out	16	B31	GND	Power	-
A32	GND	Power	-	B32	GND	Power	-

Table 3.17:	ISA XS2 (Rows C and D) Contacts Designation
-------------	---

Pin #	Signal	In/Out	LC, mA	Pin #	Signal	In/Out	LC, mA
C0	GND	Power	_	D0	GND	Power	_
C1	/SBHE	Out	8	D1	/MEMCS16	In	8
C2	LA23	Out	8	D2	/IOCS16	In	8
C3	LA22	Out	8	D3	IRQ10	In	-
C4	LA21	Out	8	D4	IRQ11	In	-
C5	LA20	Out	8	D5	IRQ12	In	-
C6	LA19	Out	8	D6	IRQ13	In	-
C7	LA18	Out	8	D7	IRQ14	In	-
C8	LA17	Out	8	D8	/DACK0	Out	8
C9	/MEMR	Out	16	D9	DRQ0	In	-
C10	/MEMW	Out	16	D10	/DACK5	Out	8
C11	SD8	In/Out	16	D11	DRQ5	In	-
C12	SD9	In/Out	16	D12	/DACK6	Out	8
C13	SD10	In/Out	16	D13	DRQ6	In	-
C14	SD11	In/Out	16	D14	/DACK7	Out	8
C15	SD12	In/Out	16	D15	DRQ7	In	-
C16	SD13	In/Out	16	D16	+5V	Power	_
C17	SD14	In/Out	16	D17	/MASTER	In	_
C18	SD15	In/Out	16	D18	GND	Power	-
C19	KEY	-	-	D19	GND	Power	-



Note:

In two tables above:

"–" – Not used;

"Power" – supplied to the stacked modules

In/Out column shows the data transfer direction for a processor module being the bus master.

3.2.13 Redundancy

CPC307 supports redundancy connection. To do so, connect the main and the reserve modules in PC/104 stack with no connection via XS1 (PCI) connector. Make connection between XP1 and XP11 pinpads according to the figure below.

Additional information on redundancy arrangement is available upon request.

Figure 3.22: Redundancy Pinpads Connection

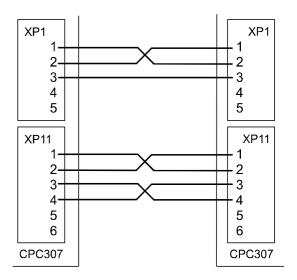


Figure 3.23: XP11 Pinpad

16Image: Image: Image:

2023-2000 contact set.

Table 3.18:	XP11 Pinout (CPC307-01)
-------------	-------------------------

Pin	Signal	Pin	Signal
1	Fail_out#	4	GPCS0#
2	Fail_in#	5	Sw_in#
3	GPCS_in#	6	GPCS1#

3.2.14 CAN Ports

Two independent CAN 2.0b interfaces of CPC307 are based on SJA1000T controllers. Both controllers can be reset by software. Base address (BA) selection is performed by programming registers of Vortex86DX SoC. Interrupt lines are hardware-defined.

Maximum transmission rate for CAN1 and CAN2 ports is 1 Mbit/s. Both ports have 500 V isolation.

Table 3.19: CAN Controllers Addresses

	CAN1	CAN2
Control area	BA+0x000 – BA+ 0x0FF	BA+0x200 – BA+ 0x2FF



Reset area (accessing these addresses leads to controller Reset)	BA+0x100 – BA+ 0x1FF	BA+0x300 – BA+ 0x3FF
ISA bus interrupt line	IRQ10	IRQ11

Details of addressing are available in Addressing section (TBA) of this document.

Figure 3.24: XP4 and XP8 Pinpads

XP4 XP8 1 2 3 4 1 2 3 4 •• •• •• •• •• •• •	120 (±5%) Ohm terminating resistors for CANL/CANH lines can be connected by setting appropriate jumpers on XP4 and XP8 pinpads. These pinpads are used also to enable the high- speed driver operation.
	speed driver operation.

Table 3.20:XP4 and XP8 Pinpads Jumpers

Closed Contacts	Connected Resistors			
XP4: 1-2	High-speed mode enabled for CAN1			
XP4: 3-4	or CANL/CANH line of CAN1			
XP8: 1-2	High-speed mode enabled for CAN2			
XP8: 3-4	Rt for CANL/CANH line of CAN2			

Figure 3.25: XP5 Pins Numbering (CAN)



CAN1 and CAN2 are routed to XP5 header (IDC2-10, 2-row, 2 mm pitch, Leotronics 2073-3102). Recommended counterpart is Leotronics 2040-3102 socket for ribbon cable or Leotronics 2022-2102 socket and 2023-2000 contact set.

Table 3.21: XP5 Connector Pinout (CAN)

Pin	Signal	Pin	Signal
1	CANH (CAN1)	2	CANL (CAN1)
3	GND_CAN1	4	-
5	-	6	-
7	-	8	CANH (CAN2)
9	CANL (CAN2)	10	GND_CAN2

3.2.15 Watchdog Timers

CPC307 has three watchdog timers.

WDT0 and WDT1 have programmable timeout period from 30.5 μ s to 512 seconds and are integrated in Vortex86DX SoC. WDT0 and WDT1 are controlled via internal processor registers. Description of these registers will be added later (*TBA*).



WDT2 has fixed timeout period of 1.6 seconds; it is integrated in ADM706T power supply supervisor chip. Expiry of its timeout period trigger special registers, which are available to BIOS function for reading after reboot. The fact of watchdog operation is also reflected by lighting HL2 green LED. WDT2 is controlled via GPIO1 port lines (1-3) of Vortex86DX. WDT2 can be disabled by setting a jumper on XP26 pinpad. See also detailed description of GPIO ports in relevant subsection of this Manual (*TBA*).

3.2.16 RTC, CMOS, Serial FRAM and Reserved BIOS

3.2.16.1 Reserved BIOS

The CPC307 takes advantage of flash-memory based BIOS. The main (working) copy of BIOS occupies 256 KB on a soldered chip. Reserve BIOS copy occupies 256 KB of flash memory integrated in the controller and is used for emergency boot.

On power-up the module is booted using main BIOS copy, if XP21 jumper is removed. If XP21 is closed and and the timeout of WDT expired, the module boots using the reserve copy.

TO enable boot using the main BIOS copy, do one of the following:

- Reset the module by pressing the SW1 (RESET#) button;
- Reset the module by an external reset, contacts 1-2 of XP25 should be closed;
- Set the jumper or close the contacts 1-2 of XP27 for a short time and then reset the module;
- Set the GPIO1 port line 3 to "0" and then reset the module;
- Switch the power off. On power-up the module will boot using the main BIOS copy.

WDT timeout expiry and the reserve BIOS copy use can be indicated by a LED connected to contacts 5-6 of XP3.

BIOS settings can be changed only in BIOS Setup utility.

3.2.16.2 RTC, CMOS and Battery

The supplied with CPC307 3 V lithium battery (CR2032) is installed in X1 holder. It is used to power the RTC and CMOS memory when the system power is off. BIOS settings are duplicated to FRAM memory and are automatically recovered in case of CMOS data loss. This allows using the module without battery; but system date and time are not stored in this case.

The capacity of the battery is 235 mA/h. The consumption current of the module in power-off state is about 2 μ A. Expected life-time of the battery is about 10 years at 23°C, but it depends on operating or storage temperature and power off time. It is recommended to replace the battery every 5 years.

Replacing the battery, observe polarity: "+" is up.

Dispose of used batteries according to the local regulations.

CMOS_RST utility is used to set BIOS parameters to default values in emergency cases. (TBA)

3.2.16.3 FRAM

FRAM is non-volatile memory with SPI interface. It serves as a back-up storage for BIOS Setup parameters and for restoration of the RTC memory (except the time and date settings) if an error is detected. This feature enables the possibility to operate the module even when the battery is disconnected. High FRAM memory units (31 KB) are available to the user via INT17H BIOS extensions. The lower 1 KB of FRAM is reserved.

FRAM can be addressed directly via SPI registers, for details, please refer to Vortex86DX and FRAM descriptions.

(TBA)

3.2.16.4 BIOS Upgrade

Reserved BIOS allows riskless upgrade of BIOS copies. Both the main and the reserve BIOS copies can be upgraded using the supplied with the module utilities.

(TBA)

3.2.17 Power Supply

The power is supplied to CPC307 via XS1 and XS2 connectors or via dedicated XP22 (AMP 4-171826-4) connector from an external power source.

Figure 3.26: XP22 Power Supply Connector



The main power voltage of the processor module is +5V \pm 5%. For stable operation of the module without external devices, the external power supply unit should provide not less than 1.2 A consumption current.

The following table gives assignments of XP22 contacts.

Table 3.22: XP22 Power Connector Pinout

Pin	Assignment
1	+5 V
2	GND
3	GND
4	-

For making a custom power cable it is recommended to use AMP 4-171822-4 socket with 170262-1 contacts.



Important:

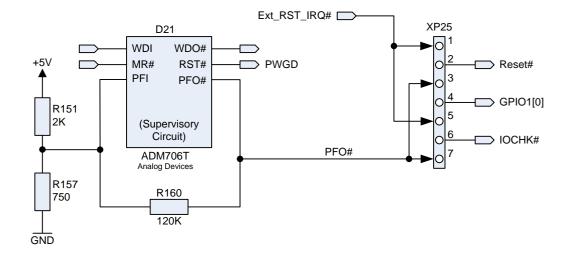
If total power consumption of PC/104 or PC/104-Plus stack exceeds 4 W, it is not allowed to power the stack via XP22 connector. In this case the power must be provided by a PC/104 power supply unit via the stack connectors.

3.2.18 Power Supply Supervisor

CPC307 is equipped with ADM706T power supply supervisor. After +5V power is supplied to the module, ADM706T generates 200 ms Reset signal (Powergood signal is set to inactive "0" level), provided that the power voltage is higher than +3.08V. If during the operation +5V voltage drops below +4.45V, then PFO# (Power Fail Output) signal is generated. This signal can be connected to different circuits using XP25 pinpad. If the voltage drops below +3.08V, then hardware Reset is issued.

See details on signal switching in Optoisolated Reset/IRQ subchapter.





3.2.19 GPIO Ports

Vortex86DX SoC includes three general purpose I/O (GPIO) ports available via internal registers. Each port consists of 8 programmable input/output lines. (*TBA*)

GPIO1 is used for watchdog timer control, as well as for switching on/off the ATA flash disk controller. GPIO2 is used for COM1, COM2 ports control, for switching user LEDs, and for reading the SA1 state. (*TBA*)

GPIO0 is available through XP14 (IDC2-10, 2-row, 2 mm pitch header; Leotronics 2073-3102). Recommended counterpart Leotronics 2040-3102 socket for ribbon cable.

(TBA)

3.2.20 Configuration Jumpers

XP4, XP8, XP15, XP18, XP20, XP21, XP24, XP25, XP26, XP27 jumpers description (TBA).

3.2.21 Diagnostic LEDs

CPC307 has three diagnostic LEDs (HL1, HL2, HL3). The following table describes the function of these LEDs.

Table 3.23:	CPC307 Diagnostic LEDs Function
-------------	---------------------------------

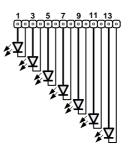
LED	Color	Function
HL1	Green	User LED controlled via GPIO2[4] line
HL2	Green	User LED controlled via GPIO2[5] line
HL3	Yellow	+5V presence

Moreover, XP3 connector is used for connection of external LEDs.



Table 3.24:	XP3 Contacts Function	
Pins	Current	Function
1 – 2	R=510, U=+5V	Ethernet Link ACT
3 – 4	R=510, U=+5V	Ethernet Duplex
5 – 6	R=330, U=+1.8V	WDO ACT
7 – 8	R=330, U=+3.3V	CPU_RESET
9 – 10	R=510, U=+5V	IDE ACT
11 – 12	R=330, U=+3.3V	USER1 (GPIO2_5)
13 – 14	R=330, U=+3.3V	USER0 (GPIO2_4)

Figure 3.28: External LEDs Connection (XP3)



3.2.22 Reset Button

In the event of a contingency (module hang-up, for example) use the Reset button SW1 on the top side of the module to reset the system.

3.3 Address Mapping

3.3.1 Memory Addressing

Table 3.25: Memory Address Mapping

Address Range	Size	Description
00000h – 9FFFFh	640 KB	System memory
A0000h – BFFFFh	128 KB	PCI/ISA VGA Graphics
C0000h – C7FFFh	32 KB	VGA BIOS
C8000h – CFFFFh	32 KB	Expansion Card Boot ROM
D0000h - EFFFFh	128 KB	Not used
F0000h – FFFFFh	64 KB	BIOS

3.3.2 I/O Addressing

Table 3.26: I/O Address Space

Address Range	Function	Note
0000h – 001Fh	8237 DMA Controller #1	-

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Address Range	Function	Note
0020h – 0021h	8259 Master Interrupt Controller	_
0022h – 0023h	Indirect Access	WDT0
0024h – 002Dh	ISA bus	External bus access
002Eh – 002Fh	Reserved	No access
0030h – 003Fh	ISA bus	External bus access
0040h – 0043h	8253 Programmable Timer	
0044h – 0047h	ISA bus	External bus access
0048h – 004Bh	Reserved	No access
004Eh – 005Fh	ISA bus	External bus access
0060h – 0064h	8042 Keyboard Controller	
0065h	WDT0	
0066h	ISA bus	External bus access
0067h – 006Dh	WDT1	_
006Eh – 006Fh	ISA bus	External bus access
0070h – 007Fh	RTC, NMI Mask Register	_
0080h – 009Fh	DMA Page Registers	
00A0h - 00B1h	8259 Slave Interrupt Controller	
00B2h – 00BFh	ISA bus	External bus access
00C0h – 00DFh	8237 DMA Controller #2	
00E0h – 01EFh	ISA bus	External bus access
01F0h – 01F8h	Primary IDE Controller	
01F9h – 0277h	ISA bus	External bus access
01F9h - 0277h 0278h - 027Fh	LPT Port	
		(possible designation)
0280h – 02E7h	ISA bus	External bus access
02E8h - 02EFh	Serial Port 4	(possible designation)
02F0h - 02F7h	ISA bus	External bus access
02F8h – 02FFh	Serial Port 2	(possible designation)
0300h – 0377h	ISA bus	External bus access
0378h – 037Fh	LPT Port	(possible designation)
0380h – 03AFh	ISA bus	External bus access
03B0h – 03BBh	MDA Adapter	(possible designation)
03BCh – 03BFh	LPT Port	(possible designation)
03C0h – 03CFh	EGA, VGA Adapter	(possible designation)
03D0h – 03DFh	CGA Adapter	(possible designation)
03E0h – 03E7h	ISA bus	External bus access
03E8h – 03EFh	Serial Port 3	(possible designation)
03F0h – 03F7h	Floppy Controller #1	(possible designation)
03F8h – 03FFh	Serial Port 1	(possible designation)
0400h – 04CFh	ISA bus	External bus access
04D0h – 04D1h	Reserved	No access
04D2h – 0777h	ISA bus	External bus access
0778h – 077Fh	Reserved	No access
0780h – 0CF7h	ISA bus	External bus access
0CF8h – 0CFFh	Host PCI controller configuration registers	
0D00h – EDFFh	ISA bus	External bus access
EE00h – EF3Fh	Reserved	No access
EF40h – FBFFh	ISA bus	External bus access
FC00h – FC0Dh	Reserved	No access
FC0Eh – FFEFh	ISA bus	External bus access

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Address Range	Function	Note	
FFF0h – FFFFh	Reserved	No access	

3.3.3 Integrated Address Decoder

Two SJA1000T CAN controllers and the controller of two RS232 ports (XR16C2850IM) require base addresses and address ranges to be set before use. For addressing these controllers two integrated in Vortex86DX address decoders are used: GPCS0 and GPCS1 (General Purpose Chip Select) lines.

(TBA)

- 3.3.3.1 CAN Ports Addresses
- (TBA)
- 3.3.3.2 COM5 and COM6 Ports Addresses

(TBA)

3.3.4 Interrupt Settings

By default, interrupts are generated by the devices belonging to the CPC307 module. The table below presents interrupt settings. Interrupt request configuration is performed in BIOS Setup.

										IRQ	Lines	6						
System Units		NMI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
System timer			•															
PS/2 keyboard				•														
PS/2 Mouse															•			
Cascading					•													
COM 1						0	•					0	0	0				
COM 2						٠	0					0	0	0				
COM 3						0	٠					0	0	0				
COM 4						٠	0					0	0	0				
COM 5										٠								
COM 6												٠						
CAN 1													٠					
CAN 2														٠				
LPT								٠		0								
RTC											•							
Ethernet																		•
USB										٠		٠	٠	٠				
Co-Processor																•		
IDE (Primary Ch	annel)																٠	
WDT0		0				0	0	0	0	0		0	0	0	0		0	0
WDT1		0				0	0	0	0	0		0	0	0	0		0	0
WDT2		0				0	0	0	0	0		0	0	0	0		0	0
External isolated interrupt		0				0	0	0	0	0		0	0	0	0		0	0
PC104		0				0	0	0	0	0		0	0	0	0		0	0
PCI104	INT A					0	0	0	0	0		0	0	0	0		0	0
	INT B					0	0	0	0	0		0	0	0	0		0	0
	INT C					0	0	0	0	0		0	0	0	0		0	0
	INT D					0	0	0	0	0		0	0	0	0		0	0

Table 3.27:	Interrupt Settings
-------------	--------------------

Legend:

•

0

Not allowedPossible

Default

Via IOCHK# signal of ISA bus

Changes in the distribution of hardware interrupts are made by means of BIOS only. IRQ[3..7], IRQ[9..12], and IRQ[14..15] interrupt lines are connected to PC/104 connector.



3.3.5 DMA Channels

Table 3.28: DMA Channels

	LPT Port	PC/104 Connector (ISA)
DREQ0	•	
DREQ1	0	•
DREQ2	0	•
DREQ3	0	•
DREQ5		•
DREQ6		•
DREQ7		•

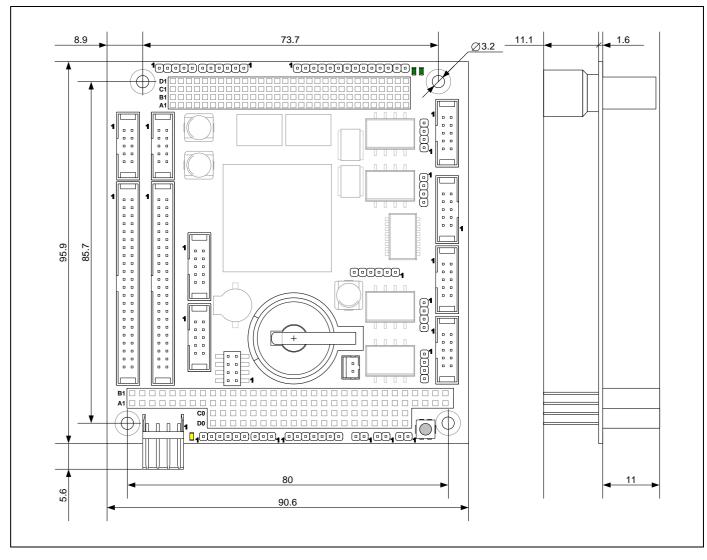
Legend:

	Not allowed
0	Possible
•	Default

Changes in the distribution of DMA requests are made by means of BIOS only. DRE[0..3] and DRE[5..7] lines are connected to PC/104 connector.



3.4 Overall and Mounting Dimensions





4 External Connections

The following precautions must be observed to ensure proper installation and to avoid damage to the module, other system components, or harm to personnel.

4.1 Safety Regulations

The following safety regulations must be observed when installing or operating the module. Fastwel assumes no responsibility for any damage resulting from infringement of these rules.



Warning!

When handling or operating the module, special attention should be paid to the heatsink, because it can get very hot during operation. Do not touch the heatsink when installing or removing the module.

Moreover, the module should not be placed on any surface or in any kind of package until the module and its heatsink have cooled down to ambient temperature.



ESD Sensitive Equipment!

This product comprises electrostatically sensitive components. Please follow the ESD safety instructions to ensure module's operability and reliability:

- Use grounding equipment, if working at an anti-static workbench. Otherwise, discharge yourself and the tools in use before touching the sensitive equipment.
- Try to avoid touching contacts, leads and components.

Extra caution should be taken in cold and dry weather.

4.2 Connection of Peripheral Devices

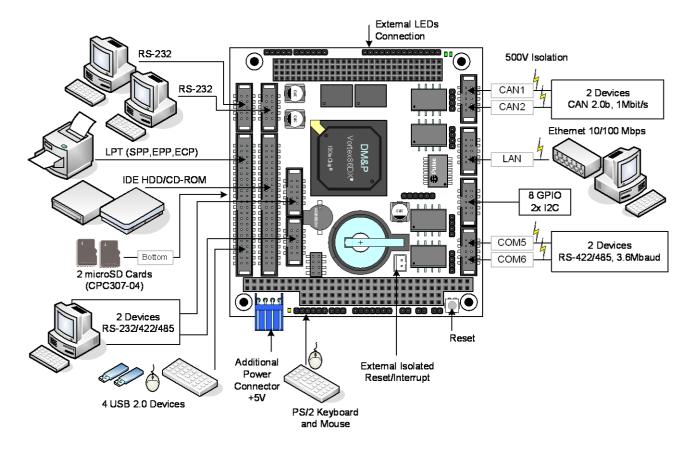
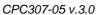


Figure 4.1: External Devices Connection



The following devices are necessary to put the module into operation:

- PC/104 power supply or an external power supply unit with +5 V and not less than 2.1 A output connected to XP22 power connector;
- A remote PC in console operation mode connected to one of COM ports (115200, 8, n, 1) selected in BIOS Setup.

The operating system is loaded from the on-board NAND Flash memory (versions -01, -02, -03, -05). Operating system on this flash-disk is FreeDOS supplemented with some service software utilities.

4.3 Software Installation

The installation of the peripheral drivers is described in the accompanying information files. For details on installation of an operating system, please refer to the relevant software documentation.



5 AMI BIOS

The AMI BIOS in CPC307 is an adapted version of a standard BIOS for IBM PC AT-compatible personal computers equipped with x86 compatible processors. BIOS provides low-level support for the central processing, memory, and I/O system units. System settings can be changed using the BIOS Setup program. The description below is for BIOS v.3.11 (CPC307 modules v.3.1). Depending on BIOS version, the number and the structure of menus may differ from the described in the following sections. Default items in the description are marked with underline.

5.1 BIOS Setup Program. Introduction

With the BIOS Setup program, you can modify BIOS settings and control special features of the module. The Setup program offers a convenient menu interface to modify basic system configuration settings and switching between the subsystems operation modes. These settings are stored in a dedicated battery-backed memory, CMOS RAM, that keeps the information while the power is switched off. For extra safety, the system settings are stored also in the nonvolatile serial FRAM.

5.2 Main Menu

To start the BIOS Setup program switch on the power or restart the system. By default the startup screen looks like this:

```
AMIBIOS(C)2006 American Megatrends, Inc.
BIOS Date: 11/02/11 17:42:32 Ver: 08.00.15
Fastwel Adaptation CPC307 BIOS V.3.11
CPU : Vortex86DX A9121
Speed : 600MHz
Press DEL to run Setup (F4 on Remote Keyboard)
Press F11 for BBS POPUP (F3 on Remote Keyboard)
Initializing USB Controllers .. Done.
256MB OK
USB Device(s): 1 Mouse
Auto-Detecting Pri Master..IDE Hard Disk
Auto-Detecting Pri Slave...IDE Hard Disk
Pri Master : 1GB ATA Flesh Disk C A254G4
Ultra DMA Mode-2, S.M.A.R.T. Capable and Status OK
Pri Slave : SMC01GBFI6E CF060926
Auto-detecting USB Mass Storage Devices ..
00 USB mass storage devices found and configured.
Checking NVRAM..
```

50AC



To start BIOS Setup, press "Del" key on a keyboard after the message

"Hit if you want to run SETUP"

appeared on the screen. This will lead you to the Main Menu screen, shown in the Figure below.



Attention!

In remote console mode the BIOS Setup utility is started by F4 on the keyboard of a remote PC with "Console Redirect" option enabled.

Figure 5.1: Main Menu Screen Image

		BIOS SET	TUP UTILITY	1.2		
Main Advance	d PCIPnP	Boot	Security	Ch	ipset	Exit
System Overview					100 - 100 - 200 - 200	ENTER], [TAB] HIFT-TAB] to
AMIBIOS Version :08.0 Build Date:11/0 ID :3BAB	2/11				selec Use [t a field. +] or [-] to gure system Time.
Processor Vortex86DX A912 Speed :600M Count :1						
System Memory Size :256M	В					Select Screen Select Item Change Field
System Time System Date		E 18 : 06 E Sun - 1	5:14] 10/19/2011]		Tab F1 F10 ESC	Select Field General Help Save and Exit
v02_6	1 (C)Copurig	of 1985-20	006. America	n Mer	ratrend	s. Inc.

The Main Menu items and their functions are described in the table below.

Table 5.1:	Main Menu Items

Menu Item	Description
AMIBIOS (info field)	 BIOS version information: Version – current BIOS core version, 08.00.14 – without SMI support, 08.00.15 – with SMI support; Build Date – BIOS release date; ID – BIOS ID
Processor (info field)	CPU information: <i>Vortex86DX A9121</i> – version of Vortex86DX rev.D; <i>Speed</i> – processor clock speed; <i>Count</i> – number of processors in system, always 1
System Memory (info field)	DDR2 SDRAM system memory information: Size – system memory size, 256 MB, fixed
System Time	Current time, [h/m/s]
System Date	Current date [m/d/y]

Use "Up" and "Down" cursor keys or <Tab> key to move between menu items. <Enter> selects the item and allows to proceed with the command or opens the submenu screen.

5.3 Advanced

On selection of this Main menu item the following screen is shown:

Figure 5.2: Advanced Screen Image

BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Secur i ty	Chipset	Exit
Advanced	Settings					Options
WARNING:		rong value system to		ow sections tion.		bled abled
Embedded	NAND Flas	h	l Ena b	led]		
 IDE Co Remote 	nfiguration nfiguration Access Con nfiguration	n nfiguratio n			+- F1 F10 ESC	dw Select Item Change Option General Help Save and Exit Exit
	v02.61 ()	C)Copyrigh	t 1985-2	006, America	n Megatre	nds, Inc.

The following table presents explanations on "Advanced" menu screen.

Menu Item	Function
Embedded NAND Flash	Soldered ATA Flash Disk controller: [Enabled], [Disabled]
CPU Configuration (submenu)	Information on the processor and its internal cache memory control
IDE Configuration (submenu)	IDE devices control
Remote Access Configuration (submenu)	Console input/output settings
USB Configuration (submenu)	Settings for all USB ports

5.3.1 CPU Configuration

The menu screen is shown in the figure below.



	Fastwel	CPC307
gure 5.3: CPU Configuration Men		
	BIOS SETUP UTILITY	
Advanced		
CPU Configuration		Options
Brand String: Vortex86DX A Frequency : 600MHz	19121	Disabled Enabled
L1 Cache	[Enabled]	
Cache L1 : 16 KB		
L2 Cache	[Enabled]	
Cache L2 : 256 KB		
		<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Comur:	ght 1985-2006, Americar	1 Meratrends, Inc.

The figure shows the default settings.

Table 5.3:	CPU Configuration Menu Items
------------	------------------------------

Menu Item	Options	Description
CPU Configuration (info field)		CPU information: Brand String – CPU ID; Frequency – CPU clock speed
L1 Cache	[<u>Enabled]</u> [Disabled]	Level 1 cache memory control
L2 Cache	[<u>Enabled]</u> [Disabled]	Level 2 cache memory control



5.3.2 IDE Configuration

The menu screen is shown in the figure below. Additional information on IDE controller is available in AT Attachment with Packet Interface – 6 (ATA/ATAPI-6) standard.

Figure 5.4: IDE Configuration Menu Screen

Advanced B	IOS SETUP UTILITY	
IDE Configuration		
OnBoard PCI IDE Controller OnBoard IDE Operate Mode Primary IDE Pin Select	[Primary] [Legacy Mode] [SD Card]	Parallel IDE SD Card
 Primary IDE Master Primary IDE Slave Hard Disk Write Protect 	: [Hard Disk] : [Not Detected] [Disabled]	the status of auto detection of IDE devices.
IDE Detect Time Out (Sec) ATA(PI) 80Pin Cable Detection	[35]	<-> Select Screen up/dw Select Item +- Change Option
		F1 General Help F10 Save and Exit ESC Exit
v02.61 (C)Copyright	1985-2006, American Me	gatrends, Inc.

The figure shows the default settings.

Table 5.4: IDE Configuration Menu Items

Menu Item	Options	Description
Onboard PCI IDE Controller	[<u>Primary</u>] [Disabled]	Integrated IDE bus controller enabled Disabled
Onboard IDE Operate Mode	[Legacy Mode] [Native Mode]	IDE controller operation mode
Primary IDE Pin Select (available for CPC307-04 only)	[SD Card] [<u>Parallel IDE</u>]	SD card mode support enabled; IDE devices operation supported
Primary IDE Master (подменю)		Primary IDE Master device: information and settings
Primary IDE Slave (подменю)		Primary IDE Slave device: information and settings. The menu structure is identical to Primary IDE Master (see below)
Hard Disk Write Protect	[Enabled] [<u>Disabled]</u>	Write protection for IDE devices enabled; Write to IDE devices allowed
IDE Detect Time Out (Sec)	[0], [5], [10], [15], [20], [25], [30], <u>[35]</u>	ATA/ATAPI device detection timeout in seconds
ATA(PI) 80Pin Cable Detection	[<u>Host & Device]</u> [Host]	Detection by system and IDE devices; Detection by system only; Detection by IDE devices only. In Native mode of IDE controller this

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Fastwel		CPC307	
Menu Item	Options	Description	
	[Device]	may lead to data loss on the integrated ATA Flash disk	

Primary IDE Master/Slave

Primary IDE Master and Primary IDE Slave submenus are identical by structure. The menu screen is shown in the figure below.

Figure 5.5: Primary IDE Master Menu Screen

Primary IDE Master			t the type vice connected
Device :Hard Disk Vendor :1GB ATA Flash Disk Size :OMB LBA Mode :Supported Block Mode:Not Supported PIO Mode :4 Async DMA :MultiWord DMA-2 Ultra DMA :Ultra DMA-6 S.M.A.R.T.:Supported		and the second se	e system.
Type LBA/Large Mode	[Auto] [Auto]		Select Screen Select Item
Block (Multi-Sector Transfer)		4-	Change Option
PIO Mode	[Auto]	F1	
DMA Mode	[Auto]	F10	
S.M.A.R.T.	[Auto]	ESC	Exit
32Bit Data Transfer	[Enabled]		

The figure shows the default settings.

Menu Item	Options	Description
Туре	[Not Installed] [<u>Auto]</u> [CD/DVD] [ARMD]	Search for IDE devices disabled; Automatic detection of the connected device type; Set the device type as CD/DVD drive; Set the type as an ATAPI Removable Media Device (ZIP, LS-120)
LBA/Large Mode	[<u>Auto]</u> [Disabled]	Automatic detection of LBA Mode support; Disabled detection of LBA Mode, Large Mode is used
Block (Multi-Sector Transfer)	[<u>Auto]</u> [Disabled]	BIOS automatically detects if the Multi-Sector Transfer mode is supported at this channel. The number of sectors per block for data transfers from the disk to memory is autodetected. Multi-Sector Transfer mode is disabled for this channel. One sector of data is transferred at a time.
PIO Mode	[<u>Auto]</u> [0] [1] [2] [3] [4]	BIOS auto detects if the connected device supports PIO mode. Recommended if the supported mode is unknown. Sets PIO 0 mode. Data transfer rate is up to 3.3 MB/s; PIO 1 mode. DTR up to 5.2 MB/s; PIO 2 mode. DTR up to 8.3 MB/s; PIO 3 mode. DTR up to 11.1 MB/s; PIO 4 mode. DTR up to 16.6 MB/s



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		CFC307
Menu Item	Options	Description
DMA Mode	[Auto] [SWDMA0] [SWDMA1] [SWDMA2] [MWDMA0] [MWDMA1] [MWDMA2]	Direct Memory Access mode is autodetected. Recommended for most efficient data transfers. In BIOS v.3.12 and later UDMA0 mode is supported only; Single-word DMA modes; Multi-word DMA modes
S.M.A.R.T.	[<u>Auto]</u> [Enabled] [Disabled]	BIOS autodetects and supports the connected device. Recommended mode; Enables S.M.A.R.T. usage; Disables S.M.A.R.T. usage
32-bit Data Transfer	[<u>Enabled]</u> [Disabled]	32-bit data transfers for the connected device

5.3.3 Remote Access Configuration

The menu screen is shown in the figure below.

Figure 5.6: Remote Access Configuration Menu Screen	Figure 5.6:	Remote Access Configuration Menu Screen
---	-------------	---

	BIOS SETUP UTILITY	
Advanced		
Configure Remote Access type	and parameters	Select Remote Access type.
Remote Access Serial port number Base Address, IRQ	[Enabled] [COM1] [3F8h, 4]	ugpe .
Serial Port Mode Flow Control Redirection After BIOS POST Terminal Type VT-UTF8 Combo Key Support	[115200 8,n,1] [None] [Boot Loader] [ANSI] [Disabled]	
Sredir Memory Display Delay Terminal Display Mode Terminal Size	[No Delay] [Normal Mode] [80 X 25]	<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

The figure shows the default settings.

Table 5.6:	Remote Access Configuration Menu Items
------------	--

Menu Item	Options	Description
Remote Access	[Disabled] [<u>Enabled]</u>	Remote access disabled; Remote access enabled. Remote access parameters become available for editing.
Serial port number	[COM1]	Selection of a serial port for remote access

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CPC307

		CPC307
Menu Item	Options	Description
	[COM2] [COM3] [COM4]	
Serial Port Mode	[<u>115200 8,n,1]</u> [57600 8,n,1] [38400 8,n,1] [19200 8,n,1] [09600 8,n,1]	Data transfer rate: 115.2 kbaud, 8-bit, no parity check, 1 stop bit; 57.6 kbaud, 8-bit, no parity check, 1 stop bit; 38.4 kbaud, 8-bit, no parity check, 1 stop bit; 19.2 kbaud, 8-bit, no parity check, 1 stop bit; 9.6 kbaud, 8-bit, no parity check, 1 stop bit
Flow Control	[<u>None]</u> [Hardware] [Software]	No flow control; CTS/RTS hardware control; XON/XOFF software control
Redirection After BIOS POST	[Disabled] [<u>Boot Loader]</u> [Always]	Disable remote access after BIOS POST procedure; Remote access is active during BIOS POST and OS loading; Remote access is always active. Some operating systems may not support this option
Terminal Type	[<u>ANSI]</u> [VT100] [VT-UTF8]	Selection of a terminal type
VT-UTF8 Combo Key Support	[<u>Disabled]</u> [Enabled]	VT-UTF8 symbols support for ANSI/VT100 terminals
Sredir Memory Display Delay	[<u>No Delay]</u> [Delay 1 Sec] [Delay 2 Sec] [Delay 4 Sec]	Sets the delay after displaying the module's system memory information at a remote PC screen
Terminal Display Mode	[Normal Mode] [<u>Recorder</u> <u>Mode]</u>	Normal mode of data transmission to a remote PC; Text only
Terminal Size	[80x24] [<u>80x25]</u>	80 symbols wide, 24 lines; 80 symbols, 25 lines

5.3.4 USB Configuration

The menu screen is shown in the figure below.

Figure 5.7: USB Configuration Menu Screen

ISB Configuration	Use [ENTER], [TAB] Configures the USB 2.0 controller in
JSB Devices Enabled : None	HiSpeed (480Mbps) or FullSpeed (12Mbps).
USB 2.0 Controller Mode [F	nabled] iSpeed] nabled]
	<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

The figure shows the default settings.

Menu Item	Options	Description
Legacy USB Support	[Disabled] [<u>Enabled]</u> [Auto]	Legacy support disabled Support enabled. Recommended setting; Autodetection
USB 2.0 Controller Mode	[<u>HiSpeed]</u> [FullSpeed]	Data rate up to 480 Mbit/s Data rate up to 12 Mbit/s (USB 1.0/1.1)
USB EHCI Hand-Off	[<u>Disabled]</u> [Enabled]	BIOS support for EHCI (Enhanced Host Controller Interface) off; BIOS support for EHCI enabled

5.4 PCI Plug and Play

PCI Plug and Play menu screen is shown on the following figure:

Figure 5.8: PCI Plug and Play Menu Screen

	BIOS SET	UP UTILITY			440.523
Main Advanced PCIPnP	Boot	Secur i ty	Chi	pset	Exit
Advanced PCI/PnP Settings					r NVRAM during em Boot.
WARNING: Setting wrong value	WARNING: Setting wrong values in below sections				
may cause system to					
Clear NURAM	[No]				
Plug & Play O/S	[No]				
PCI Latency Timer Allocate IRQ to PCI VGA	[64] [No]				
	[Disal	1.41			
Palette Snooping PCI IDE BusMaster	[Disal				
OffBoard PCI/ISA IDE Card	[Auto]				
orrootra reny ion ibb cara	LINE CO.	8			
IRQ3	EReser	ued 1			
IRQ4	EReser				
IRQ5	[Avai]				
IRQ7	EReser				
IRQ9	EReser				
IRQ10	EReser	ved]			
IRQ11	EReser	ved]			
IRQ14	[Avai]	able]			
IRQ15	[Avai]	able]			
DMA Channel 0	[Avai]			<->	Select Screen
DMA Channel 1	[Avai]			**	Select Item
DMA Channel 3	[Avai]			+-	Change Option
DMA Channel 5	[Avai]			F1	General Help
DMA Channel 6	[Avai]			F10	Save and Exit
DMA Channel 7	[Avai]	lablel		ESC	Exit
Reserved Memory Size	[Disal	ledl			
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weren coverputin	10 1.200 GV	and millest state	n neg	pares estim	as j aller

The figure shows the default settings.

PCI Plug and Play menu items are described in the table below.

Menu Item	Options	Description
Clear NVRAM	[<u>No]</u> [Yes]	Do not reset PnP parameters on boot; Clear NVRAM data on every boot
Plug & Play O/S	[<u>No]</u> [Yes]	Operating system does not support PnP; OS supports PnP
PCI Latency Timer	[32], [<u>64],</u> [96], [128], [160], [192], [224],	Maximum number of PCI bus clocks that a device on bus can keep it busy sending data.



~		~~
C	PC3	SU /

		CPC307
Menu Item	Options	Description
	[248]	
Allocate IRQ to PCI VGA	[<u>No]</u> [Yes]	Do not allow to assign an interrupt to PCI graphics card
Palette Snooping	[<u>Disabled]</u> [Enabled]	Recommended. Data flow is directed to PCI VGA device only; Palette synchronization for several VGA devices is allowed
PCI IDE BusMaster	[<u>Disabled]</u> [Enabled]	Enable/disable Bus Mastering mode for PCI IDE controller
OffBoard PCI/ISA IDE Card	[Auto] [PCI Slot1] [PCI Slot2] [PCI Slot3] [PCI Slot4] [PCI Slot5] [PCI Slot6]	Autodetection of PCI/ISA IDE controller card. Recommended; Manual selection of a PCI slot for IDE controller card
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ14 IRQ15	[Available] [Reserved]	Allow the selected IRQ for usage by external PnP devices; Reserve the selected IRQ for legacy devices of Vortex86DX: IRQs 3, 4 and 7, 9, 10, 11 are reserved for COM1-COM4, COM5,6, CAN1,2. If these ports are not used, the respective interrupts may be made available for external devices.
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	[Available] [Reserved]	Allow the selected DMA channel for usage by external PnP devices; Reserve the selected DMA channel for legacy devices of Vortex86DX
Reserved Memory Size	[<u>Disabled]</u> [16k], [32k], [64k]	Do not allow BIOS to reserve memory for ISA bus devices; Reserve the selected memory size for ISA devices
To correct pos	sible errors, resta	lead to abnormal system performance. rt the BIOS Setup program and restore manufacturer's settings factory defaults" command in Main menu.

5.5 Boot Options

Boot menu screen is shown on the following figure:

Figure 5.9: Boot Menu Screen

		(A) (PAC) R	BIOS SE	TUP UTILITY		20020-012
Main	Advanced	PCIPnP	Boot	Secur i ty	Chipset	Exit
Boot Se	ettings					gure Settings g System Boot.
▹ Boot	Settings Ca	mfiguratio			uurrn	g agatem boot.
	nt Device Int Device			PS-1GB ATA F PM-SMC01GBF1	A State of the second	
						Select Item
					F1	
					F10 ESC	
-		C)Conuniak	+ 1995_2	006, America	n Maratnend	e Inc

The figure shows the default settings.

Boot menu items are described in the table below.

Table 5.9: Boot Menu Items

Menu Item	Options	Description
Boot Settings Configuration (submenu)		See description of the submenu below
1st Boot Device		By default boot from the selected device
2nd Boot Device 		The module is booted from this device if the first device is not bootable (and so on). After the first connection of an USB drive or after changes in configuration, the module is booted from an USB drive

5.5.1 Boot Settings Configuration

The menu screen is shown in the figure below.

Figure 5.10: Boot Settings Configuration Menu Screen

Boot Settings Configuration	Allows BIOS to skip	
Quick Boot Add On ROM Display Mode Bootup Num-Lock PS/2 Mouse Support Wait For 'F1' If Error Hit 'DEL' Message Display Interrupt 19 Capture	[Enabled] [Force BIOS] [On] [Auto] [Disabled] [Enabled] [Enabled]	— certain tests while booting. This will decrease the time needed to boot the system.
		<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

The figure shows the default settings.

Table 5.10: Boot Settings Configuration Menu Items

Menu Item	Options	Description
Quick Boot	[Disabled] [<u>Enabled]</u>	Full system self check on power up; Reduced number of tests allows to speed up booting
Add On ROM Display Mode	[Force BIOS] [Keep Current]	Expansion cards BIOS information is shown on monitor during the system loading; System displays only POST information during loading
Bootup Num-Lock	[Off] [<u>On]</u>	Num Lock off after loading; Num Lock on
PS/2 Mouse Support	[Disabled] [Enabled] [<u>Auto]</u>	PS/2 mouse support; Support autodetected. Recommended setting
Wait for 'F1' If Error	[<u>Disabled]</u> [Enabled]	Select this option only if the cause of a BIOS error is known; Wait for "F1" key pressing on boot error
Hit 'DEL' Message Display	[Disabled] [<u>Enabled]</u>	"Hit DEL to enter Setup" message is not displayed during boot up; "Hit DEL to enter Setup" message displayed
Interrupt 19 Capture	[Disabled] [<u>Enabled]</u>	Capture of INT19 by additional controllers is not allowed; Capture of INT19 is allowed

5.6 Security Options

Security menu screen is shown on the following figure:

Figure 5.11: Security Menu Screen

		BIOS SE	TUP UTILITY		
Main Advanced	l PCIPnP	Boot	Security	Ch	ipset Exit
Security Setting	ß				Install or Change the password.
Supervisor Passu User Password	ord :Not Ins :Not Ins				pussion u .
Change Supervise Change User Pass					
Boot Sector Viru	is Protection	EDisa	bled]		
					<-> Select Screen
					up/dw Select Item Enter Change
					F1 General Help F10 Save and Exit ESC Exit
02.6				M	ratrends. Inc.

Table 5.11: Security Menu Items

Menu Item	Options	Description
Change Supervisor Password		Password for loading the system. It is requested during POST
Change User Password		The password for entering BIOS Setup
Boot Sector Virus Protection	[Disabled] [<u>Enabled]</u>	If any program (or virus) attempts to format a disk or tries to write to boot sector a warning is shown at screen. When an attempt to write to boot sector detected, the following messages are displayed: Boot Sector Write! Possible VIRUS: Continue (Y/N)?_ It is possible that you will need to press "N" several times to prevent writing to boot sector. Any attempt to format a disk via BIOS INT 13 Hard disk drive Service leads to the following messages: Format!!! Possible VIRUS: Continue (Y/N)?_

5.7 Chipset Menu

The menu screen is shown in the figure below.

Figure 5.12: Chipset Menu Screen Image

			BIOS SE	TUP UTILITY		
Main	Advanced	PCIPnP	Boot	Security	Chipset	t Exit
Advance	ed Chipset S	Settings				tions for NB
→ Nort	G: Setting w may cause hBridge Conf hBridge Conf	: system to iguration				
					up/ Eht F1 F1	 Select Screen /dw Select Item ter Go to Sub Screen General Help Save and Exit C Exit
	v02.61 (C)Copyrigh	t 1985-2	006, America	n Megatre	ends, Inc.

The figure shows the default settings.

Table 5.12:Chipset Menu Items

Menu Item	Options	Description	
NorthBridge Configuration (submenu)		Access to North bridge settings (see below)	
SouthBridge Configuration (submenu) Access to South bridge settings			
Remember! Wrong or incorrect settings may lead to abnormal system performance.			

emember! Wrong or incorrect settings may lead to abnormal system performance. To correct possible errors, restart the BIOS Setup program and restore manufacturer's settings by selection of "Reset CMOS to factory defaults" command in Main menu.

5.7.1 North Bridge Configuration

The menu screen is shown in the figure below.

Figure 5.13: North Bridge Configuration Menu Screen

		Chipset
NorthBridge Chipset Confi	SDRAM Timing Setting Control.	
CPU Speed Setting DRAM Timing Setting CAS Latency tWR tRFC tRP tRCD	[Devide By 1] [Manual] [3 CLKs] [4 CLKs] [38] [4 CLKs] [4 CLKs] [4 CLKs]	 Control. By BIOS: Set timings by hard coding values in BIOS. By Manual: Set timings by Setup Options. <-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit

Table 5.13: North Bridge Configuration Menu Items

Menu Item	Options	Description
CPU Speed Setting	[<u>Devide by 1]</u> [Devide by 2] [Devide by 8]	Recommended setting for clock divider; Settings 28 are not supported
DRAM Timing Setting	[<u>BIOS]</u> [Manual]	Automatic settings for DDR2 SDRAM. Recommended; Manual configuration

5.7.2 South Bridge Configuration

The menu screen is shown in the figure below.

Figure 5.14: South Bridge Configuration Menu Screen

	BIOS SETUP UTILITY	ł	
		Chipset	
South Bridge Chipset C	onfiguration	USB Controller Enab	le
USB Port 0,1	[Enabled]		
USB Port 2,3	[Enabled]		
SB LAN	[Enabled]		
MAC Address 00 08 B3 A	A 00 11		
ISA Configuration	0 0		
Serial/Parallel Port WatchDog Configurati			
GPID and I2C Configu			
Hi-speed UART and CA		<-> Select Screen	5
- III speca oniti ana on	ar contrigutation	up/dw Select Item	
		+- Change Option	6
		F1 General Help	
		F10 Save and Exit	e.
		ESC Exit	
v02.61 (C)Co	pyright 1985-2006, Americ	can Megatrends, Inc.	

Table 5.14: South Bridge Configurat	tion Menu Items
-------------------------------------	-----------------

Menu Item	Options	Description
USB Port 0,1	[<u>Enabled]</u> [Disabled]	USB ports 0 and 1 control
USB Port 2,3	[<u>Enabled]</u> [Disabled]	USB ports 2 and 3 control
SB LAN	[<u>Enabled]</u> [Disabled]	Integrated Ethernet (LAN) controller enabled; Integrated Ethernet (LAN) controller disabled
MAC Address (info field)		MAC-address of the integrated Ethernet controller
ISA Configuration (submenu)		ISA bus settings: frequency, timings (TBA)
Serial/Parallel Port Configuration (submenu)		Addresses, modes, and interrupts for serial and parallel ports (TBA)
WatchDog Configuration (submenu)		Settings for integrated watchdog timers (WDT0 and WDT1) (TBA)
GPIO and I2C Configuration (submenu)		GPIO[0] input/output port settings (TBA)
CAN and COM5,6 Configuration (submenu)		Settings for CAN1,2 and COM5,6 ports (TBA)

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5.7.2.1 ISA Configuration

View of the "ISA Configuration" menu screen is shown in Fig. 5.15, description of menu items is given in Table 5.15.

Fig. 5.15:	"ISA Configuration" menu screen
------------	---------------------------------

9	BIOS SETUP UTILITY			
	Chipset			
ISA Clock ISA 16bits I/O wait-state ISA 8bits I/O wait-state ISA 16bits Memory wait-state ISA 8bits Memory wait-state	[4 clock] [1 clock]	Options 8.3MHz 16.6MHz		
		<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit		

Table 5.15: Description of the "ISA Configuration" menu

Menu item	Purpose			
ISA Clock	Clock frequency of ISA_SYSCLK (CLK, connector XS2, output B20)			
	[8.3MHz] Set the clock frequency 8 MHz			
	[16.6MHz] Set the clock frequency 16 MHz			
ISA 16bits I/O wait-state	Time of I/O wait-state cycle at 16-bit addressing on ISA bus			
	[1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock], [8 clock]			



Menu item	Purpose		
ISA 8 bits I/O wait-state	Time of I/O wait-state cycle at 8-bit addressing on ISA bus		
	[1 clock], [2 clock], [3 clock], [<u>4 clock]</u> , [5 clock], [6 clock], [7 clock], [8 clock]		
ISA 16bits Memory wait- state	Time of the Memory wait-state cycle at 16-bit addressing on ISA bus.		
	[0 clock], [1 clock], [2 clock], [3 clock], [4 clock], [5 clock], [6 clock], [7 clock]		
ISA 8bits Memory wait-	Time of the Memory wait-state cycle at 8-bit addressing on ISA-bus.		
state	[1 clock], [2 clock], [3 clock], [<u>4 clock</u>], [5 clock], [6 clock], [7 clock], [8 clock]		

5.7.2.2 Serial/Parallel Port Configuration

View of the "Serial/Parallel Port Configuration" menu screen is shown in Fig. 5.16, description of menu items is given in Table 5.16.

Fig. 5.16: View of the "Serial/Parallel Port Configuration" menu tab

	Chipset		
Serial Port IRQ 2 Serial Port Boud Rate SB Serial Port 3 Serial Port IRQ 3 Serial Port Boud Rate SB Serial Port 4 Serial Port IRQ 4 Serial Port Boud Rate	[115200 BPS] [2F8] [IRQ3] [115200 BPS] [3E8] [IRQ4] [115200 BPS] [2E8] [IRQ3] [IRQ3] [115200 BPS] [378]	Allows BIOS to Select Parallel Port Base Addresses.	



Table 5.16: Description of the "Serial/Parallel Port Configuration" menu

Menu item	Purpose			
SB Serial Port 1 SB Serial Port 2	This option assi	gns address for the relevant serial port (for each port individually)		
SB Serial Port 3	[Disabled]	Port operation is prohibited		
SB Serial Port 4	[3E8]	Assigning 3E8h I/O base address		
	[2E8]	Assigning 2E8h I/O base address		
	[3F8]	Assigning 3F8h I/O base address		
	[2F8]	Assigning 2F8h I/O base address		
Serial Port IRQ 1 Serial Port IRQ 2 Serial Port IRQ 3	This option assign (for each port in	gns an interrupt line for the relevant serial port dividually)		
Serial Port IRQ 4	[IRQ3]	Assigning interrupt line IRQ3		
	[IRQ4]	Assigning interrupt line IRQ4		
	[IRQ9]	Assigning interrupt line IRQ9		
	[IRQ10]	Assigning interrupt line IRQ10		
	[IRQ11]	Assigning interrupt line IRQ11		
Serial Port Baud Rate	This option sets the speed of data exchange for the relevant serial port (for each port individually)			
	[2400 BPS], [48 BPS]	00 BPS], [9600 BPS], [19200 BPS], [38400 BPS], [57600 BPS], [115200		
SB Parallel Port Address	This option assigns address for LPT1 parallel port			
	[Disabled]	Port operation is prohibited		
	[<u>378]</u>	Assigning 378h I/O base address		
	[278]	Assigning 278h I/O base address		
Parallel Port Mode	This option sets	operation mode for LPT1 parallel port		
	[BPP]	"Bi-directional Parallel Port" (BPP) operation mode Receive/transmit data mode for parallel port		
	[EPP 1.9 AND SPP]	Operation mode, compatible with EPP 1.9 and SPP modes.		
	[ECP]	"Enhanced Capabilities Port" (ECP) operation mode ECP uses DMA protocol for achieving the data transfer speed up to 2,5 Mb/sec. ECP ensures symmetrical, bidirectional data exchange		
	[ECP AND EPP 1.9]	Operation mode, compatible with ECP and EPP 1.9 modes		
	[SPP]	"Standard Parallel Port" (SPP) operation mode		
	[<u>EPP 1.7 AND</u> SPP] 	Operation mode, compatible with EPP 1.7 and SPP modes. The "Enhanced Parallel Port" (EPP) operation mode uses existing signals of parallel port for asymmetric bidirectional data transfer from the master device		
	[ECP AND EPP 1.7]	Operation mode, compatible with ECP and EPP 1.7 modes		
Parallel Port IRQ	This option assig	gns an interrupt line for LPT1 parallel port		
	[IRQ5]	Assigning interrupt line IRQ5		
	[IRQ7]	Assigning interrupt line IRQ7		

5.7.2.3 WatchDog Configuration

View of the "Watchdog Configuration" menu screen is shown in Fig. 5.17, description of menu items is given in Table 5.17.



В	BIOS SETUP UTILITY Chipset		
WatchDog 1 Function WatchDog 1 Signal Select	[64 Sec] [Enabled]	Options Enabled Disabled <-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit	
v02.61 (C)Comuright	1985-2006, American Me	matrends. Inc	

Table 5.17: Description of the "WatchDog Configuration" menu

Menu item	Purpose		
WatchDog 0 Function WatchDog 1 Function	Operation control of WDT0, WDT1 watchdog timers integrated into Vortex86DX SoC		
5	[Disabled]	Timer operation is disabled	
	[Enabled]	Timer operation is enabled	
WatchDog 0 Signal Select WatchDog 1 Signal Select	This option makes it possible to determine an action that will be selected upon completion of the counting time of the relevant watchdog. Generation of one of the interrupts is possible, including a non-maskable interrupt, as well as shaping a module reset signal. [IRQ3], [IRQ4], [IRQ5], [IRQ6], [IRQ7], [IRQ9], [IRQ10], [IRQ11], [IRQ12], [IRQ14],		
WatchDog 0 Timer WatchDog 0 Timer	watchdog timer to 0 and then w timer obtains a from 64	punting time interval of the relevant timer. During operation counts backwards. If you set the value as 64 seconds, it will count ill shape RESET, NMI or IRQ signal. If during the countdown, the reboot signal, it interrupts the counting and starts to count again [4 Sec], [8 Sec], [16 Sec], [32 Sec], [64 Sec], [128 Sec],	

5.7.2.4 GPIO and I2C Configuration

View of the "GPIO and I2C Configuration" menu screen is shown in Fig. 5.18, description of menu items is given in Table 5.18.

Fig. 5.18: View of the "GPIO and I2C Configuration" menu screen

	BIOS SETUP UTILITY Chipset			
GPIO PORTO 78H [30] FUNC GPIO PORTO 78H [30] DATA	[]]]] [0000]	Options 2xI2C Bus		
GPIO [74] & IZC Pin Select GPIO PORTO 78H [30] DATA	[1111]	GPIO [74]		
GPIO PORTO 78H [30] DATA	[0000]			
		<-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit		
v02.61 (C)Copyright	1985-2006, American Me	gatrends, Inc.		

Table. 5.18: Description of the "GPIO and I2C Configuration" menu

Menu item	Purpose			
GPIO PORT0 78H [30] FUNC	Configuring port lines to "input" or "output" states. Each line can be individually set as input or output.			
	[<u>* *]</u>	The line is set as "input"		
	[*0*]	The line is set as "output"		
GPIO PORT0 78H [30] DATA	Setting output lines of the port to log.1 or log.0. states Each line can be set to log.1 or.0 regardless of the states of their lines			
	[*1*]	The line is set to log.1 state (+3.3V)		
	[<u>*0*]</u>	The line is set to log.0 state		
GPIO PORT0 78H [74] & I2C	Selection of operation mode of [74] GPIO 0 port			
Pin Select	2xI2C Bus	Two I2C ports		
	GPIO [74]	Lines of GPIO 0/O port		
GPIO PORT0 78H [74] FUNC	NC Configuring port lines to "input" or "output" states. Each line can be individually "input" or "output"			
	[* *]	The line is configured as "input"		
	[*0*]	The line is configured as "output"		
GPIO PORT0 78H [74] DATA	A Setting output lines of the port to log.1 or log.0. states Each line can be set to l regardless of the states of their lines			
	[*1*]	The line is set to log.1 state (+3.3V)		
	[*0*] The line is set to log.0 state			



5.7.2.5 CAN and COM5,6 Configuration

View of the "CAN and COM5,6 Configuration" menu screen is shown in Fig. 5.19, description of menu items is given in Table 5.19.

Fig. 5.19: View of the "CAN and COM5,6 Configuration" screen menu

B	Chipset	
CAN Function CAN Base Address COM5 / COM6 Function COM5 / COM6 Base Address	[Enabled] [DF000] [Enabled]	Options Enabled Disabled <-> Select Screen up/dw Select Item +- Change Option F1 General Help F10 Save and Exit ESC Exit
υθ2 61 (C)Conuringht	1995 2006 Anonioan	Menatrends. Inc

 Table 5.19: Description of the "CAN and COM5,6 Configuration" menu

Menu item	Purpose			
CAN Function	Control of CAN1, CAN2 ports operation			
	[Enabled] Address decrypting is on, the ports are available for programming			
	[Disabled] Address decrypting is off, the ports are available for programming			
CAN Base Address	Specifying base address for CAN1, CAN2 ports. 4x base addresses are available: [CE000], [CF000], [DE000], [DF000]			
COM5 / COM6 Function	Control of COM	5, COM6 ports operation		
	[Enabled] Address decrypting is on, the ports are available for programming			
	[Disabled] Address decrypting is off, the ports are available for programming			
COM5 / COM6 Base Address	Specifying base address for COM5, COM6 ports. 4x base addresses are available: [220 / 228], [240 / 248], [320 / 328], [340 / 348]			

5.8 Exit Menu

The figure below presents the Exit menu screen.

Figure 5.20: Exit Menu Screen Image

Main	Advanced	PCIPnP	BIOS SE Boot	TUP UTILITY Security	Chipset	Exit
Exit O				obsar rug	Exit	t system setup
Discar Discar	hanges and E d Changes an d Changes ptimal Defau	d Exit			chai F10	er saving the nges. key can be used this operation.
					up/d Ehte F1 F10	Select Screen W Select Item er Go to Sub Screen General Help Save and Exit Exit
	v02.61 (C)Conur inh	t. 1985-2	006, America	n Meratrer	uds. Inc.

Table 5.20: Exit Menu Items

Menu Item	Description
Save Changes and Exit	Save settings in CMOS and FRAM memory and leave BIOS Setup
Discard Changes and Exit	Leave BIOS Setup without saving changes in CMOS and FRAM
Discard Changes	Discard the changes of BIOS settings without leaving BIOS Setup
Load Optimal Defaults	Load optimal (factory) settings without leaving BIOS Setup

5.9 Functional Constraints of BIOS Versions

BIOS v.3.12 (Core Version 8.00.15, created 31/01/2012) preinstalled in version 3.1 modules, has the following functional constraints:

- 1. Corrected skipping of Autoexec.bat at the command Ctrl+B from a remote PC.
- 2. Corrected remote operation via COM2.
- 3. IDE port operation mode is limited to UDMA0 to provide system operation stability when working with different IDE devices under extreme ambient temperatures.

BIOS v.3.11 (Core Version 8.00.15, created 11/02/2011) in version 3.1 modules:

1. Remote operation via COM2 is not functional. COM1, 3, 4 are recommended for remote PC operation.

BIOS v.2.0 (Core Version 8.00.15, created 01/20/2010) in version 3.0 modules:

- In «Native Mode» of IDE controller when «PCI IDE BusMaster Enabled» and «ATA(PI) 80Pin Cable Detection – Device» options are set, ATA Flash disk may not operate correctly.
- BIOS v.1.1 of (Core Version 8.00.14, created 11/24/2009) in version 2.0 modules:
 - 1. DMA on IDE bus is not supported (fixed in BIOS v.2.0).
 - 2. USB keyboards and mice are not supported (fixed in BIOS v.2.0).
 - 3. Slow loading when only one IDE device is connected (fixed in BIOS v.2.0).

ANNEX A: BIOS update

BIOS redundancy mechanism makes it possible to remotely update BIOS primary copy which will not lead to module breakdown in case of updating failure (due to power loss, downloading of invalid BIOS image file etc.).

Relevant BIOS image file versions for CPC307 module can be downloaded from the following link: http://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC307/

The BIOS primary copy is stored in the chip of parallel FLASH-memory, connected to ISA bus - AM29F040B-55EF memory chip, 4 Mb Flash Memory.

Backup copy is stored in the FLASH-memory, integrated to CHK Vortex86DX and connected to SPI-interface. The backup copy is designed for repairing of the damaged primary copy of BIOS (e.g. in case of BIOS updating failure).

When BIOS is updated with the use of integrated console I/O (p. 5.2.3 Remote Access Configuration (Console I/O settings)), it is required to consider the fact that after image update and reboot, the optimal (factory) BIOS Setup settings will be loaded. If the module is rebooted from the changed BIOS version to the previous one, the optimal (factory) BIOS Setup settings will also be loaded. In both cases, the console I/O settings will be changed to the factory settings (Mode "Redirection After BIOS POST" = "Boot Loader"). Therefore, if the integrated console I/O should be used, then each time the module is booted during the BIOS update procedure, it is required to enter BIOS Setup and adjust the required settings for the console I/O and BIOS, in general. It is allowed to use the console I/O, OS resources, in order not to change the BIOS Setup setting each time, which will facilitate the updating procedure of the both BIOS copies.

In order to update primary and then backup BIOS copy it is required to install XP21 jumper and not to install XP26 jumper (p. 4.3.21 Configuration jumpers).

In order to update the primary BIOS primary copy it is required to perform the following actions:

1. Switch on CPC307 and start it in the standard mode from BIOS primary copy.

2. Copy VXDXBIOS folder to the module's boot disk from the following link:

<u>ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC307/Software/BIOS/DOS/</u>. The updated BIOS image (e.g. file c307v310.bin) should be placed into such a copied folder.

3. Run the program of the BIOS primary copy update from VXDXBIOS folder. Name of the BIOS image file for update should be specified as a parameter:

C:\VXDXBIOS\vxdxbios.exe c307v311.bin

In case of a successful update, the program will show the following messages:

Load file C:\VXDXBIOS\c307v311.bin... START FLASH ERASE FLASH ERASE OK. ERASE TIME 4.62 S FLASH WRITE OK FLASH VERIFY OK AM29F040B loaded successfully

4. After update of BIOS primary copy, it is necessary to restart the module. In order to do that you need to first switch off the module's power supply and then switch it back on, or press SW1 reset button, or reset the module by using an opto-isolated reset signal.

After module reboot, optimal (factory) BIOS Setup settings can be loaded. If necessary, you should enter BIOS Setup, change the required parameters, save the changes and exit (p. 5.7 Exit).

5. You need to make that the module has been booted right from BIOS primary copy:

a. XP21 jumper is installed and XP26 jumper is removed. WDT2 watchdog timer should not be activated during the booting process (p. 4.3.16.2 WDT2 watchdog timer). Make sure that the WDT2 watchdog timer was not actuated; it can be done using LED-indicators connected to XP3 (p. 4.3.22 LEDs). BIOS release date and version can also be checked during POST procedure and in BIOS Setup menu (p. 5 Basic I/O system (BIOS)).

b. XP21 jumper is removed or XP21 and XP26 jumpers are simultaneously installed. The module is always booted from the primary copy. If the module was booted, it means that the updating has been successful.

If the module was booted from BIOS primary copy, it means that the updating has been successful.

For updating of BIOS backup copy, it is required to perform the following actions:

1. Install XP21 jumper, and not to install XP26 jumper. Otherwise, it is impossible to update the backup copy.

2. Switch on CPC307 and boot it in the standard mode from BIOS primary copy. WDT2 watchdog timer should not be actuated during the booting process (p. 4.3.16.2 WDT2 watchdog timer). Make sure that the WDT2 watchdog timer was not actuated; it can be done using LED-indicators connected to XP3 (p. 4.3.22 LEDs). BIOS release date and version can also be checked during POST procedure and in BIOS Setup menu (p. 5 Basic I/O system (BIOS)).

If the module is not booted from BIOS primary copy, updating of BIOS backup copy is not allowed. 3. Copy SPIFLASH folder to module's boot disk from the following link:

<u>ftp://ftp.prosoft.ru/pub/Hardware/Fastwel/CPx/CPC307/Software/BIOS/DOS/</u>. The updated BIOS image (e.g. file c307v310.bin) should be placed to such copied folder.

4. Make sure that XP21 jumper is installed. XP26 jumper should be removed.

5. Start WDTRST.EXE to activate WDT2 watchdog timer and reboot using BIOS backup copy (stored at SPIFLASH folder).

C:\SPIFLASH\wdtrst.exe

After the module's reboot, optimal (factory) BIOS Setup settings can be loaded. If necessary, enter BIOS Setup, change the required parameters, save the changes and exit (p. 5.7 Exit).

6. Start the program of BIOS backup copy update from SPIFLASH folder with "u" key and specify the BIOS updated image:

C:\SPIFLASH\spiflash.exe u c307v311.bin

In case of successful update, the program will show the following messages:

SPIFLASH 1.11 (May 21 2008)

(C) Copyright 2007 DMP Electronics Inc.

CPU name = Vortex86DX

SPI base address = fc00

send RDID cmd

Device ID=c2 20 15

Flash type = MX25L1605, ok

Update flash rom data from c307v311.bin:

ADDR: 40000/40000

189 blank data block(s) skipped

Ok

7. After updating of BIOS backup copy it is required to start WDTRST.EXE, in order to repeatedly reboot the module from the BIOS backup copy and check the update accuracy.

After the module's reboot, optimal (factory) BIOS Setup settings can be loaded. If necessary, you should enter BIOS Setup, change the required parameters, save the changes and exit (p. 5.7 Exit). If the module was booted, it means that the BIOS backup copy has been successfully updated. If the update of the primary BIOS copy resulted in an error and the module can't be booted (information on the executed POST procedure is not shown and the console output was switched on) or WDT2 watchdog timer is actuated (XP26 jumper is removed, module is reset at regular intervals), it is required to:

1. Install XP21 jumper and remove XP26 jumper.

2. Switch on CPC307 and boot the module from BIOS backup copy (if BIOS primary copy is damaged, WDT2 watchdog timer will be actuated).

After the module's reboot, optimal (factory) BIOS Setup settings can be loaded. If necessary, you should enter BIOS Setup, change the required parameters, save the changes and exit (p. 5.7 Exit).

3. Start the program of BIOS primary copy update from the VXDXBIOS folder. The file name of BIOS image should be specified as a parameter for updating: C:\VXDXBIOS\vxdxbios.exe c307v311.bin

In case of successful update, the program will show the following messages: Load file C:\VXDXBIOS\c307v311.bin... START FLASH ERASE FLASH ERASE OK. ERASE TIME 4.62 S FLASH WRITE OK FLASH VERIFY OK AM29F040B loaded successfully

6. After update of BIOS primary copy it is required to reboot the module. In order to so, just switch off the module's power supply then switch it back on, or press SW1 reset button, or reset the module by using an opto-isolated reset signal. Additionally, XP21 jumper can be removed, in order to prevent switching to BIOS backup copy.

After the module's reboot, optimal (factory) BIOS Setup settings can be loaded. If necessary, you should enter BIOS Setup, change the required parameters, save the changes and exit (p. 5.7 Exit).

7. It is necessary to make sure that the module has been booted from BIOS primary copy: a. XP21 jumper is installed and XP26 jumper is removed. WDT2 watchdog timer can't be actuated during the booting process (p. 4.3.16.2 WDT2 watchdog timer). In order to make sure that the WDT2 watchdog timer has not been actuated, you can use LED indicators, connected to XP3 (p. 4.3.22 LEDs). You can also check BIOS release date and version during POST procedure and in BIOS Setup menu (p. 5 Basic I/O system (BIOS)).

b. XP21 jumper is removed or XP21 and XP26 jumpers are installed simultaneously. Module is always booted from the primary copy. If the module is loaded, the update was successful.

If the module was loaded from BIOS primary copy it means the update was successful. If BIOS backup copy is damaged and the module is not booted from the backup copy or the WDT2 watchdog timer is actuated (XP21 jumper is installed), in order to restore BIOS backup copy you'll need to send the module to repairs specifying the reason "BIOS backup copy is damaged".

ANNEX:B DISCLAIMER

This Disclaimer contains special operating conditions of Fastwel in the following areas: intellectual property, warranty policy, conditions of the order and delivery.

1 INTELLECTUAL PRORETY

1.1 If any infraction, interference, improper use, illegitimate exploitation and/or violation of the industrial and/or intellectual property rights of any third party and/or property, exploitation during the use of Fastwel Embedded Module will take place – Fastwel does not guarantee to replace the materials, computer programs, procedures or equipment affected by the complaint and under no circumstances doesn't bear responsibility in any form for possible refusal in case of such a replacement.

1.2 Use of the Fastwel products as well as the objects of intellectual property containing in them, in the ways and for the purposes, not provided by the present user manual and datasheet isn't allowed without preliminary written approval of Fastwel.

1.3 Fastwel is not responsible for possible incidents and losses, related to the operation of end devices, in which the original Fastwel equipment is used.

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2.1 When the detected flaws in an element can be corrected without decreasing the foreseen technical features and functionality for it, User may demand Fastwel the urgent correction of the failures in additionally agreed period and an increasing of the period of the guarantee of the element equal as the time elapsed from the formal request to repair the failures, until the receipt of the repaired element. All costs associated to the correction of failures, included those of assembly, dismantle, transport, tests, etc, if they exist, shall be prosecuted according the Warranty Policy of Fastwel.

3 ORDER AND DELIVERY CONDITIONS

3.1 The general rule is that all Fastwel equipment prices are determined with due consideration of delivery under the EXW terms and conditions (Incoterms 2010). Delivery of the products under other terms and conditions should be preliminary agreed and stated in writing between the parties.

3.2 Unless otherwise expressly agreed with Fastwel, all the deliveries of Fastwel equipment will be carried out only after the official purchase order is obtained and provided that the ordered products have been prepaid in full. Other terms and conditions of cooperation should be made in writing.

3.3 Any delivery of Fastwel electronics is submitted with the right package in accordance with the current rules and standards in the Member States of the European Economic Area. The purchaser independently bears all risks regarding the compliance of package and marking of Fastwel products with legislation requirements being in effect at the place of purchased products destination (in the buyer's country). The specified condition excludes unequivocally any liability of Fastwel for possible non-compliance of package and marking of products with the requirements of legislation of the country of products destination.

3.4 In general, all components of the supply are properly protected with respect to freight, in order to avoid any damage to the supply, third parties, environmental damages or unrelated goods, as consequence of wrong packaging.

3.5 Each package unit is labeled on the exterior area with the indications of product's Part Number and Serial Number.

3.6 The support documents for the order should be made either in English or in Russian unless otherwise agreed between parties in writing.

3.7 Fastwel does not pay penalties and does not cover costs associated with delay in the delivery of the products caused by actions of the third parties, force-majeure etc. - Fastwel doesn't bear any responsibility for non-execution or inadequate execution of the obligations in a case when it is caused by actions of the third parties (for example producers or suppliers of accessories), force majeure etc.

3.8 Fastwel declares that independently and at any time without damage, it has an exclusive right to define and change functionality architecture, bill of materials of its products without any preliminary coordination and approvals of the third parties.

4 OTHER CONDITIONS

4.1 Fastwel has the obligation to respect the current Russian legislation (including, but not limited to environmental, labor, social laws) in each moment and to apply it to its embedded electronics considering all and each execution phase, that is to say, from the design until the commissioning and subsequent maintenance. In this regard Fastwel is not liable to the user or other persons in connection with possible changes of the company's rules (including, but not limited to warranty, ordering policy) caused by changes of the Russian legislation.

4.2 Unless otherwise expressly agreed in writing, Fastwel provides no training for assembly\installation\adjustment\operation of its equipment.